SOLID STATE MINI-RPV COLOR IMAGING SYSTEM

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General Electric Company

Prepared for:

Aeronautical Systems Division
Advanced Research Projects Agency

12 September 1975

SOLID STATE MINI-RPV

COLOR IMAGING SYSTEM

SEPTEMBER 12, 1975

GENERAL ELECTRIC COMPANY
AEROSPACE ELECTRONIC SYSTEMS DEPT.
UTICA, NEW YORK

SPONSORED BY

ADVANCED RESEARCH PROJECT AGENCY
ARPA ORDER NO. 2713

AND

ASD (DEPUTY FOR RECONNAISSANCE, STRIKE, AND ELECTRONIC WARFARE)
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE

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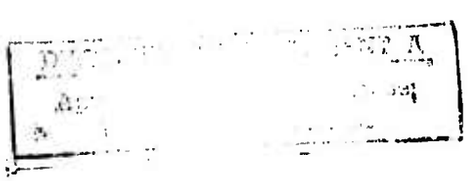
Approved by:

9/5/75
Date



REPORT SUMMARY

The general purpose of the project was to utilize solid state sensors in the development of a false color camera compatible to packaging and interface constraints of the Aequare RPV.

The first task was to develop a Charge Injection Device in a 244 x248 (vertical x horizontal) array configuration. This device, in turn, was used as the sensor for a three sensor false color camera which was designed and constructed compatible to the Aequare configuration. Finally, since a significant aspect of the Charge Injection Device, is its potential for random access, a study was done to predict performance parameters for the case of a randomly accessible device. All tasks have been completed with deliverable hardware being represented by the Color Camera and a Color Monitor.

The random access study emphasized operational timing constraints and was conducted by considering an actual layout for a 128 x 128 array with projections to a 256 x 256 array.

All tasks have been completed in the design and construction phase. Considerations are now in progress for conducting field tests of the equipment against "real world" targets.

TABLE OF CONTENTS

Section		Page
I.	INTRODUCTION	
	1.1 Introduction	1-1
II.	OPERATION	
	2.1 General Description	2-1
	2.2 Optics	2-11
	2.3 Sensors A1, A2, A3	2-18
	2.4 Drivers A4 and Oscillator A5	2-29
	2.5 Preamplifier A6	2-35
	2.6 FPN Canceler A9	2-41
	2.7 Color Processor A7	2-49
	2.8 Color Encoder A8	2-56
	2.9 Plug-In Matrix Design	2-67
III.	REPLACEMENT PARTS LIST	
	3.1 Organization	3-1
	• CID Color Camera	3-4
	• Sensor A1, A2, A3	3-5
	• Oscillator A5	3-6
	• Drivers A4	3-7
	• Preamplifier A6	3-11
	• Color Processor A7	3-14
	• Encoder A8	3-19
	• FPN Canceler A9	3-24
IV.	SCHEMATIC DIAGRAMS	4-1
V.	ASSEMBLY DIAGRAMS	5-1
APPENDIX 1	RANDOM ADDRESSING OF THE CID IMAGER	A1-1
APPENDIX 2	TEST RESULTS	A2-1

LIST OF ILLUSTRATIONS

Figure	Title	Page
1-1	CID Camera in Aequare Configuration	1-3
2-1	CID Camera Block Diagram	2-2
2-2	Servo Timing Diagram	2-5
2-3	CID Camera Optics	2-12
2-4	Prism Spectral Transmission	2-14
2-5	CID Array Spectral Response	2-15
2-6	Spectral Characteristics	2-17
2-7	Raster Scan CID Array	2-19
2-8	Simplified Parallel Injection Configuration	2-21
2-9	CID Parallel Injection Configuration	2-23
2-10	Element Rate Timing	2-25
2-11	Horizontal Input and Phase Line Timing	2-26
2-12	Line Reset/Injection Timing	2-27
2-13	Line Rate Timing (Start of Readout)	2-28
2-14	Driver A4 Block Diagram	2-31
2-15	Element Scan Time Base	2-33
2-16	Preamplifier Input Timing	2-36
2-17	Preamplifier, Single Channel Block Diagram	2-37
2-18	Double Sampler	2-38
2-19	Preamplifier Sampler and Multiplexer Timing	2-40
2-20	Single Channel of FPN Canceler, Simplified Block Diagram	2-42
2-21	Single Channel of FPN Canceler, Detailed Block Diagram	2-47
2-22	Color Processor A7 Block Diagram	2-51

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
2-23	Chromaticity Chart	2-57
2-24	Chrominance Phase	2-59
2-25	Encoder Block Diagram	2-62
2-26	Gamma Corrector Simplified Schematic	2-63
2-27	Node Voltages as a Function of Input	2-64
2-28	Typical Current Input for 4 x 6 Matrix Column	2-69
4-1	Interconnection Diagram (SK56079-21-6)	4-2
4-2	Sensor Schematic Diagram (SK56079-21-7)	4-3
4-3	Driver Schematic Diagram (SK56079-21-8) (2 sheets)	4-4
4-4	Timing Interconnection Table (SK56079-21-26) (2 sheets)	4-6
4-5	Preamplifier Schematic Diagram (SK56079-21-10)	4-8
4-6	FPN Canceler Schematic Diagram (SK56079-21-13)	4-9
4-7	Color Processor Schematic Diagram (SK56079-21-11) (2 sheets)	4-10
4-8	Encoder Schematic Diagram (SK56079-21-12)	4-12
4-9	Plug-In Matrix Schematic Diagram (SK56079-21-14)	4-13
5-1	CID Camera Assembly Drawing (SK56079-21-16)	5-2
5-2	Driver Assembly Drawing (SK56079-21-18)	5-3
5-3	Preamplifier Assembly Drawing (SK56079-21-20)	5-4
5-4	FPN Canceler Assembly Drawing (SK56079-21-23)	5-5
5-5	Color Processor Assembly Drawing (SK56079-21-21)	5-6
5-6	Encoder Assembly Drawing (SK56079-21-22)	5-7

LIST OF TABLES

Table	Title	Page
2-1	Subassemblies of CID Camera	2-3
2-2	Sensor Channel Assignments	2-8
2-3	CID Camera Interface	2-24
2-4	Odd Field Sequence, FPN Canceler	2-44
2-5	Line Format for Interlaced Display	2-45
3-1	Vendor Abbreviations, Address and Codes	3-2

SECTION I

INTRODUCTION

1.1 INTRODUCTION

This report describes the solid state false color camera (CID Camera) developed by the General Electric Company on Contract F33615-C-74-2048.

The program need was based on the evolving requirements for television sensors for use on remotely piloted vehicles. Several factors entered into these considerations. First, solid state sensors should provide cameras which are economical, reliable, and low in power consumption and weight. Secondly, the available long wavelength response of silicon sensors provides spectral information which can be used for discrimination purposes. Finally, the potential of the Charge Injection Device (CID) to be randomly addressed provides growth opportunity whereby this characteristic can be used for readout modes which can further reduce peripheral functions for modes of operation, such as, tracking or the inclusion of bandwidth compression techniques.

Based on the above, the goals of the contract were to develop a Charge Injection Device solid state sensor in a 244x248 array and to incorporate this device into a three channel multispectral television camera capable of field flight test evaluation.

1.1 (Continued)

Camera packaging and design is compatible with the size constraints of the Aequare RPV. The camera was installed and tested in a simulated Aequare configuration as shown in figure 1-1 to demonstrate design compatibility.

The developed arrays are sequentially scanned as opposed to randomly accessed. However, a study was done to determine the timing constraints anticipated for randomly accessible devices. Results are contained in Appendix 1.

The camera has been completed as described in the following material with the next logical step being field evaluation.

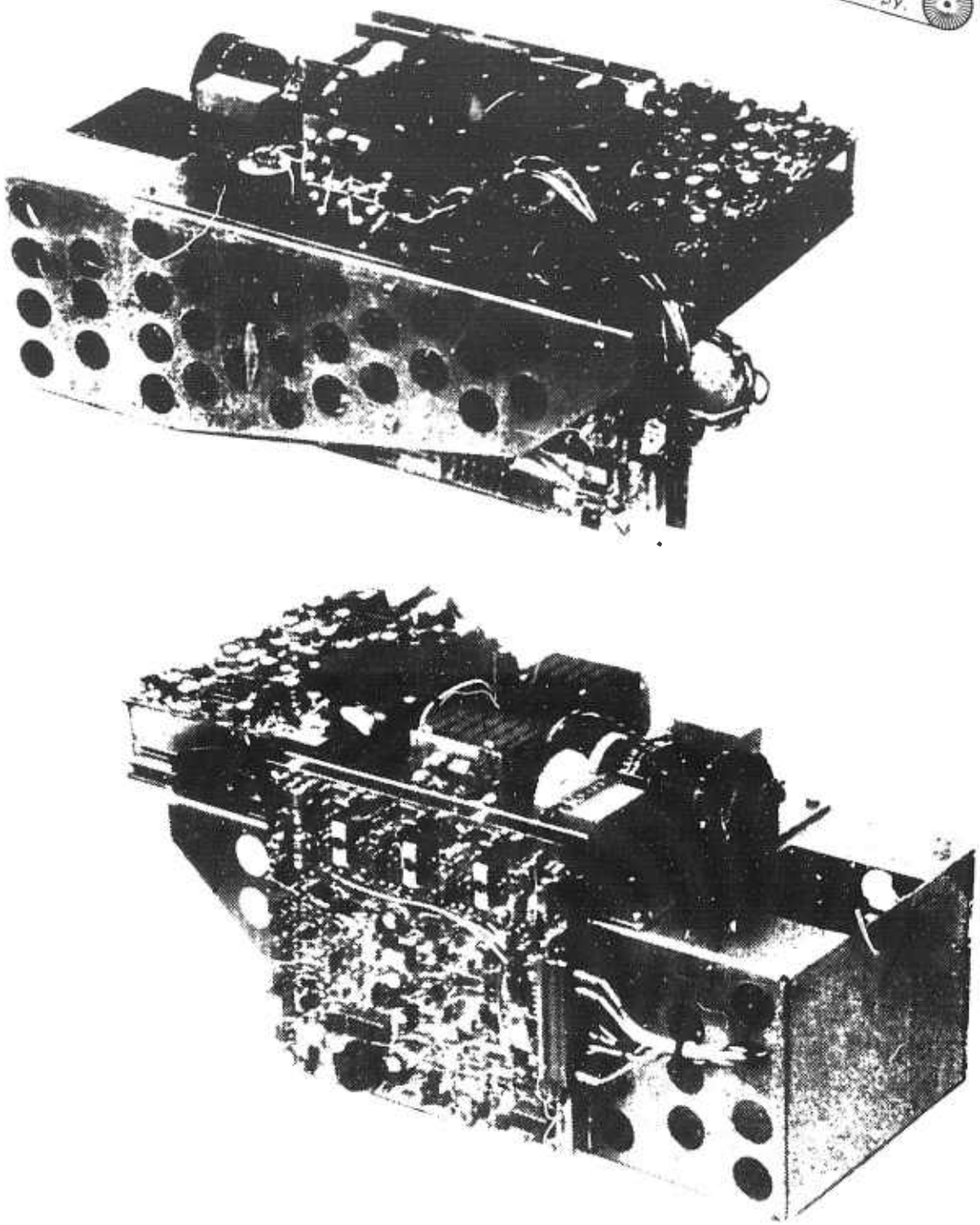


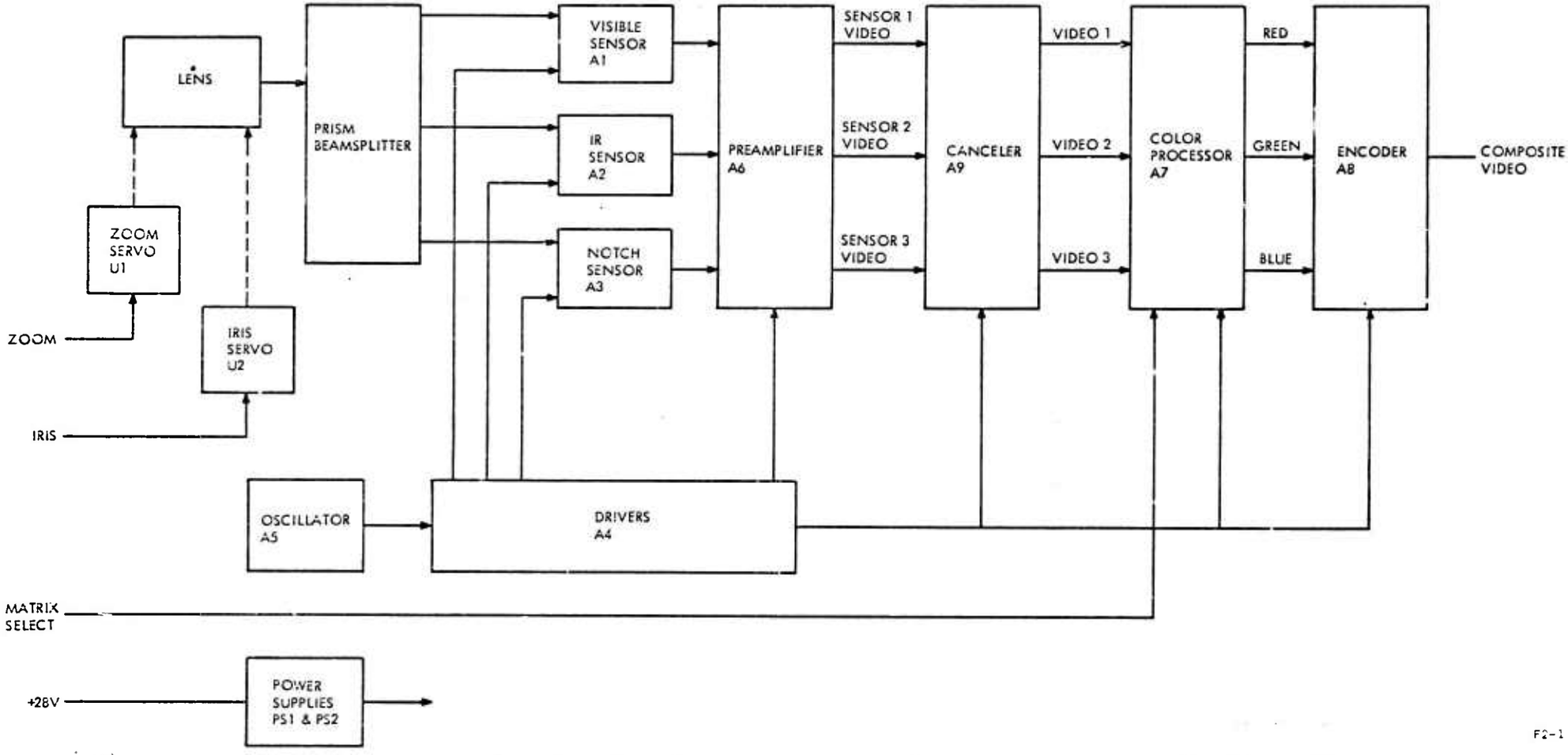
Figure 1-1. CID Camera in Aequare Configuration

SECTION II

OPERATION

2.1 GENERAL DESCRIPTION

The overall block diagram of the CID Camera is shown in Figure 2-1. This section briefly discusses the function of each subassembly shown. Later sections give the detailed circuit descriptions and input/output specifications of the individual subassemblies. Table 2-1 shows the subassemblies of the CID color camera, with cross references to the schematic diagram (Section IV) and the assembly diagram (Section V). Replacement parts lists are given in Section III and are referenced by title and reference designator.



F2-1

Figure 2-1. CID Camera Block Diagram

TABLE 2-1. SUBASSEMBLIES OF CID CAMERA

TITLE	REFERENCE DESIGNATOR	DESCRIPTION PARAGRAPH	SCHEMATIC DIAGRAM SKETCH	SCHEMATIC DIAGRAM FIGURE	ASSEMBLY DIAGRAM SKETCH	ASSEMBLY DIAGRAM FIGURE
CID CAMERA	-	2.1	SK56079-21-6	4-1	SK56079-21-16	5-1
SENSOR	A1,A2,A3	2.3	SK56079-21-7	4-2	--	--
DRIVER	A4	2.4	SK56079-21-8 SK56079-21-26	4-3 4-4	SK56079-21-18	5-2
OSCILLATOR	A5	2.4	P/O SK56079-21-6	4-1	--	--
PREAMPLIFIER	A6	2.5	SK56079-21-10	4-5	SK56079-21-20	5-3
FPN CANCELER	A9	2.6	SK56079-21-13	4-6	SK56079-21-23	5-4
COLOR PROCESSOR	A7	2.7	SK56079-21-11	4-7	SK56079-21-21	5-5
COLOR ENCODER	A8	2.8	SK56079-21-12	4-8	SK56079-21-22	5-6
PLUG IN MATRIX	A7A1,A7A2	2.9	SK56079-21-14	4-9	--	--

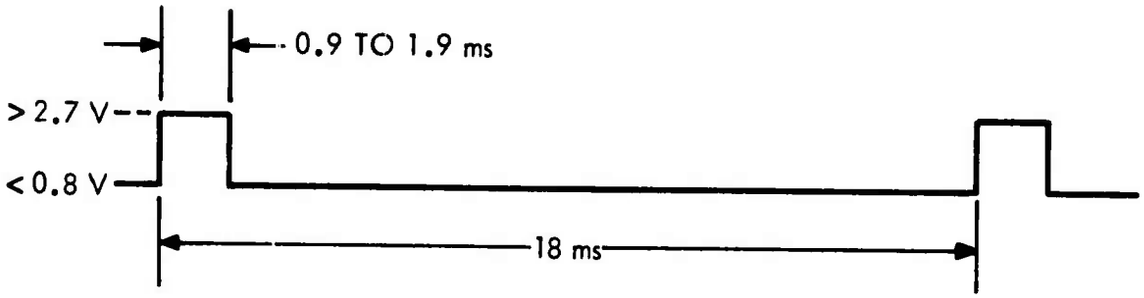
2.1.1 CAMERA INTFRFACE

INPUTS:

+28V	28V ± 1V at 1.6 ampere
ZOOM SERVO	TTL Level, Figure 2-2
IRIS SERVO	TTL Level, Figure 2-2
SERVO +5	5V at 0.8a (intermittent)
MATRIX SELECT	>2.7V Matrix A2 selected
	<0.8V Matrix A1 selected

OUTPUTS:

COMPOSITE VIDEO	1 VPP, Black negative, into 75 Ω
	Timing and Chroma encoding compatible
	with NTSC standards
+5V Out	5V at 1a (auxilary power for servo
	controls)



ZOOM SERVO	MIN PULSEWIDTH = 19° FOV
	MAX PULSEWIDTH = 4.8° FOV
IRIS SERVO	MIN PULSEWIDTH = f/7.6
	MAX PULSEWIDTH = f/44

F2-2

Figure 2-2. Servo Timing Diagram

2.1.2 THEORY OF OPERATION

The optical chain in figure 2-1 functions to spectrally separate and focus the scene on the three CID sensors which are discussed in more detail later. In general, however, the first element is a lens with remotely controllable zoom and iris. This is followed by a relay lens which magnifies and projects the image of the scene through spectrally selective prisms to the three CID sensors. Facility is incorporated for inclusion of ND Filters between the relay lens and prism should they be found desirable.

Basic optical parameters are:

f/#		7.6 to 44
focal length		34 to 170mm
Image Sensor diag.		14.26mm
FOV:	NARROW	4.8 degree diagonal
	WIDE	19.0 degree diagonal

2.1.2 (Continued)

The camera electronics shown in figure 2-1 include all of the necessary circuitry to control the CID, extract video from the CID output, and encode the three color signals for transmission over a single telemetry channel. The composite video output is compatible with NTSC standards to permit display on an unmodified color monitor.

Since this is a "false" color camera, the three optical paths, VISIBLE, NOTCH and IR, do not directly correspond to the three video signals displayed as RED, GREEN, AND BLUE. The relationship is given by the matrix equation

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{21} & A_{23} \\ A_{31} & A_{31} & A_{33} \end{bmatrix} \begin{bmatrix} V1 \\ V2 \\ V3 \end{bmatrix} \qquad (1)$$

where

R = Red Video

G = Green Video

B = Blue Video

V1 = Video 1 (Visible)

V2 = Video 2 (IR)

V3 = Video 3 (Notch)

The matrix operation occurs in the color processor. Prior to that, the video signals are denoted by number according to Table 2-2.

2.1.2 (Continued)

Table 2-2. Sensor Channel Assignments

	SENSOR	CHANNEL
VISIBLE	A1	VIDEO 1
IR	A2	VIDEO 2
NOTCH	A3	VIDEO 3

The three CID image sensors are mounted on individual circuit boards, A1, A2, and A3 in their respective image planes behind the prism beam-splitters. The CID's have 248 elements per row with 244 rows. Each row is displayed twice each frame to match the 484 unblanked lines of the standard 525 line 2:1 interlaced format. An element scan rate of 4.772727 MHz reads the 248 elements in 51.96 usec. Their rate was chosen to be 4/3 of the color subcarrier frequency to permit use of a common high frequency oscillator (A5) at 14.31818 MHz. All camera timing is synchronous with this clock.

2.1.2 (Continued)

The CID sensors require eleven MOS level drives, along with several DC biases. These are provided by the Drivers subassembly A4. In addition, the synchronizing signals necessary for the operation of the other camera electronics are provided by A4.

The outputs from each of the three sensors are applied to the preamplifier A6, which contains three identical channels. The preamplifier employs double sampling to extract the video information and reject the clock line interference. Double sampling also eliminates the 1/f noise from the on-chip preamplifier stage in the CID.

The outputs from the three channels of the preamplifier contain interference and a low frequency shading component. This undesired additive noise is virtually identical on each display line, and has a magnitude of 1/2 of signal level. The Canceler A9 uses a one-line delay along with a double read technique to subtract the fixed pattern noise on one line from the next, thus reducing the noise by 26db. The canceler also blanks the video to establish a clean black reference.

The Color Processor A7 contains a 40 db automatic gain control on each sensor channel. The gains of each AGC are matched to maintain color balance with varying light levels. The processor also performs the matrixing function described earlier. Two separate matrices may be remotely selected by means of the TTL level input MATRIX SELECT. The actual two sets of matrix coefficients are determined by the plug-in assemblies A7A1 and A7A2.

2.1.2 (Continued)

The Encoder A8 combines the RED, GREEN, and BLUE VIDEO with composite sync and blanking to form composite video compatible with the standards established by the National Television Systems Committee (NTSC). Bandwidths different from NTSC standards have been incorporated to simplify the design while permitting the use of a NTSC compatible monitor.

The power supplies PS1 and PS2 are purchased parts. The loads are separated such that the digital circuits, i.e. the drivers, are on PS2 and the analog circuits, which comprise the remainder of the camera, are on PS1. This isolates the heavy transient loads of the driver board from the analog circuits.

2.2 CAMERA OPTICS

The camera optics are shown in figure 2-3. The function of the optics is to spectrally separate the scene and selectively image spectral bands on each of three Charge Injection Devices (CID's).

Aequare payload packaging constraints limit the lens diameter to a maximum of 1.9 inches. Based on this, the previously used Monital 130/109 lens with diameter of 1.78 inches was selected. This lens has the desirable zoom and iris controls with adequate focal length for a narrow field of view. As a component, the Monital lens has a focal length range from 17 to 85mm, an aperture range from f/3.8 to f/22, and a transmission of approximately 70%. The image plane is 0.69 inches from the rear mounting flange.

Two aspects of this lens require the addition of a relay lens. First, its intended use is for a 16mm picture frame with a 12.5mm diagonal, whereas, the CID diagonal is 14.26mm. Secondly, the 0.69 inch back focal distance is not adequate to project the image through the 1.146 inch prisms and subsequently on to the CID's located behind the prisms.

The relay lens consists of a 25mm lens followed by a 50mm lens. The first lens is positioned such that its focal plane coincides with the image plane of the zoom lens. The light between the two elements is collimated and the output image lies on the focal plane of the second lens. The result is an image magnification of two and an increase in back focal length sufficient to accommodate the prisms. The combination of the zoom lens and relay lens results in an effective doubling of both the f/# and the focal length as compared to using the zoom lens alone. The transmission of the relay lens is approximately 70%.

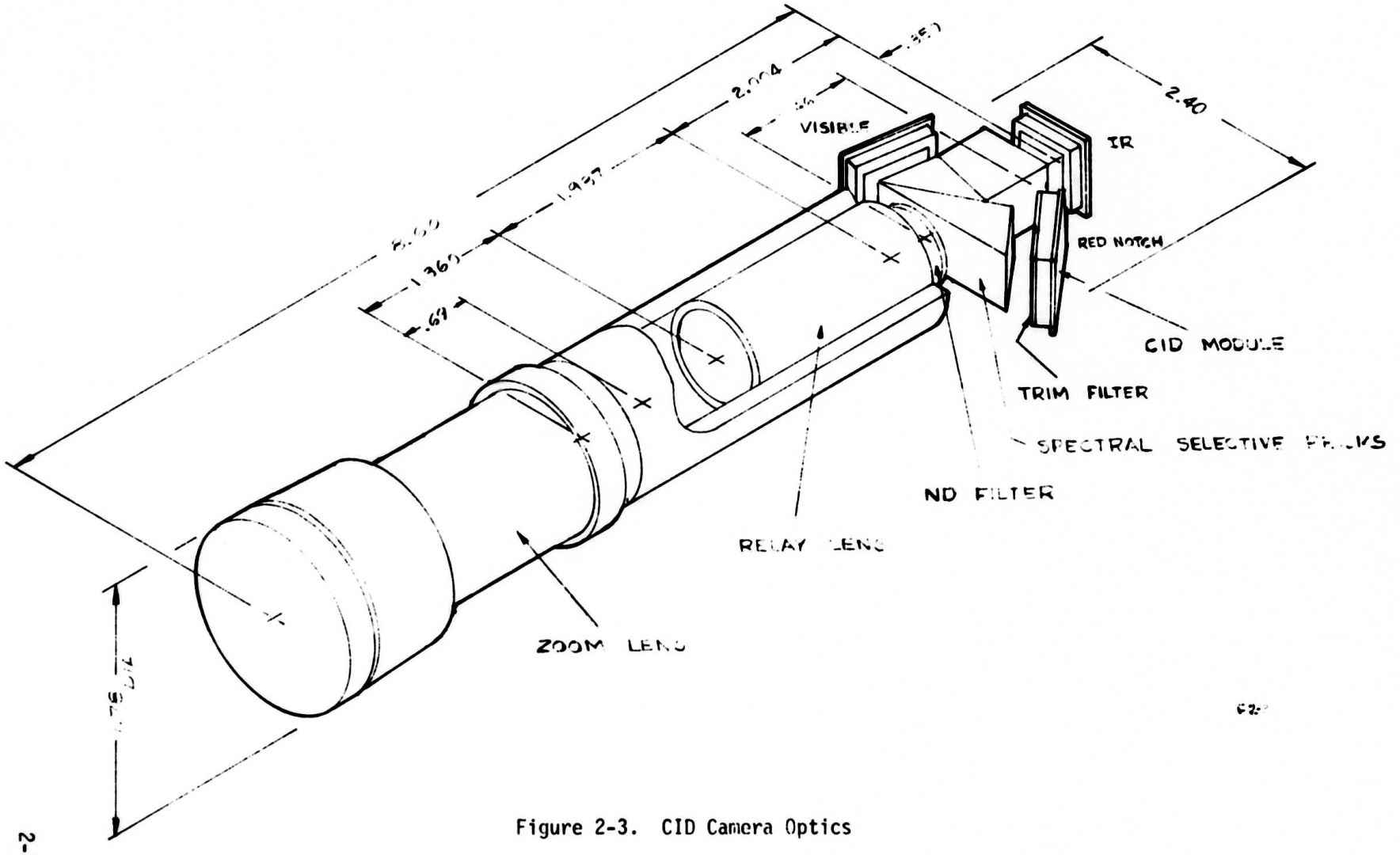


Figure 2-3. CID Camera Optics

2.2 (Continued)

The result is an optical system with the following characteristics:

Focal length	34 to 170mm
f/#	7.6 to 44
Transmission	50%

Field of view (FOV) (when used with 14.26mm diagonal CID and a 4:3 aspect ratio)

NARROW:

Diagonal	4.8 degrees
Horizontal	3.84 degrees
Vertical	2.88 degrees

WIDE:

Diagonal	23.7 degrees (independent of Aequare sight)
Diagonal	19 degrees (with Aequare sight)

The next element in the optical chain is the facility for incorporating an ND filter for the case where illumination levels are beyond the range of the iris. The need for illumination attenuation is not anticipated in the current configuration and a 1mm coated clear glass occupies the space such that focus will not be affected should a filter be added.

The ND filter is followed by a set of spectrally selective prisms which separates the image into spectral bands for display on the CID's. An RG590 trim filter is used in conjunction with the red notch channel to eliminate a small level of short wavelength energy which otherwise transmits through the prism. Characteristics of the combination are shown in figure 2-4.

Finally the prisms are followed by the Charge Injection Devices, the spectral response of which is shown in figure 2-5.

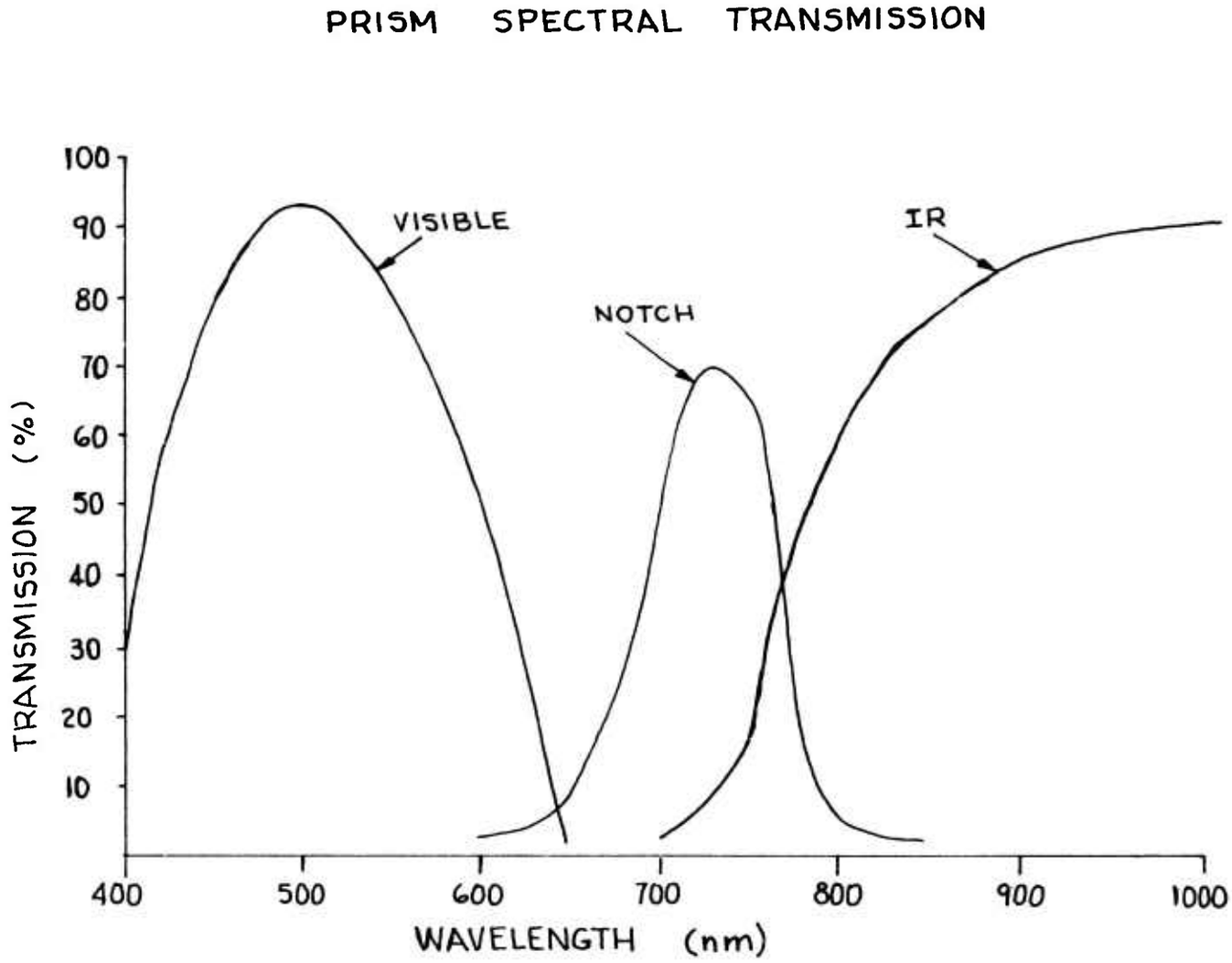


Figure 2-4. Prism Spectral Transmission

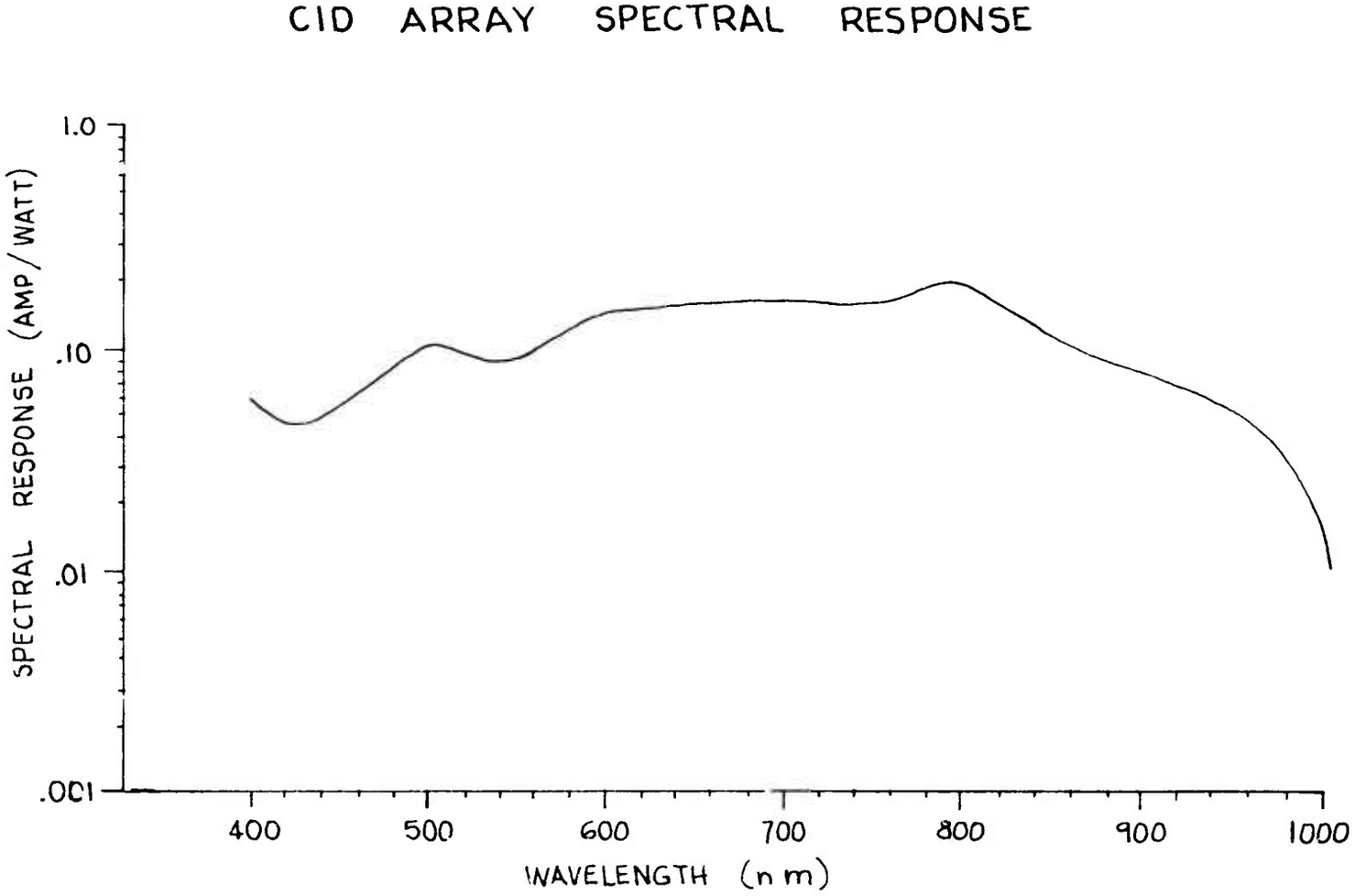


Figure 2-5. CID Array Spectral Response

2.2 (Continued)

Figure 2-6 illustrates several other spectral characteristics of interest. Since primary camera use is considered to be under daylight conditions, irradiance is considered to be that which is available from sunlight on a clear day through one air mass. A curve of sunlight irradiance is provided in units of watts per 10 nanometers per square meter. Although the curve appears to drop off slightly over 900 nanometers, data is available and was considered to 1000 nanometers. The remainder of this figure contains reflective characteristics of several potential targets of interest.

The adequacy of the optics with a 50% transmission and an f/# of 7.6 was a concern. Calculations were made based on the irradiance, reflectance, transmission, and response curves of this section. Based on an integration time of 1/30 second and a pixel saturation charge of 0.17 picocoulomb, the available current per pixel was calculated with the lens of f/7.6. The following table contains the ratio of available current to saturation current.

	VISIBLE	NOTCH	IR
SAND	3.4	3.3	4.7
ROAD	1.7	1.8	3.4
VEGETATION	1.3	3.0	5.6
TRUCK	0.55	1	2.4

It can be seen that although the optics do not have a great deal of margin, they are adequate. Real world camera operation confirmed the above, in that, under clear day sunlight conditions, approximately two f stops were required to operate the device below saturation.

SPECTRAL CHARACTERISTICS

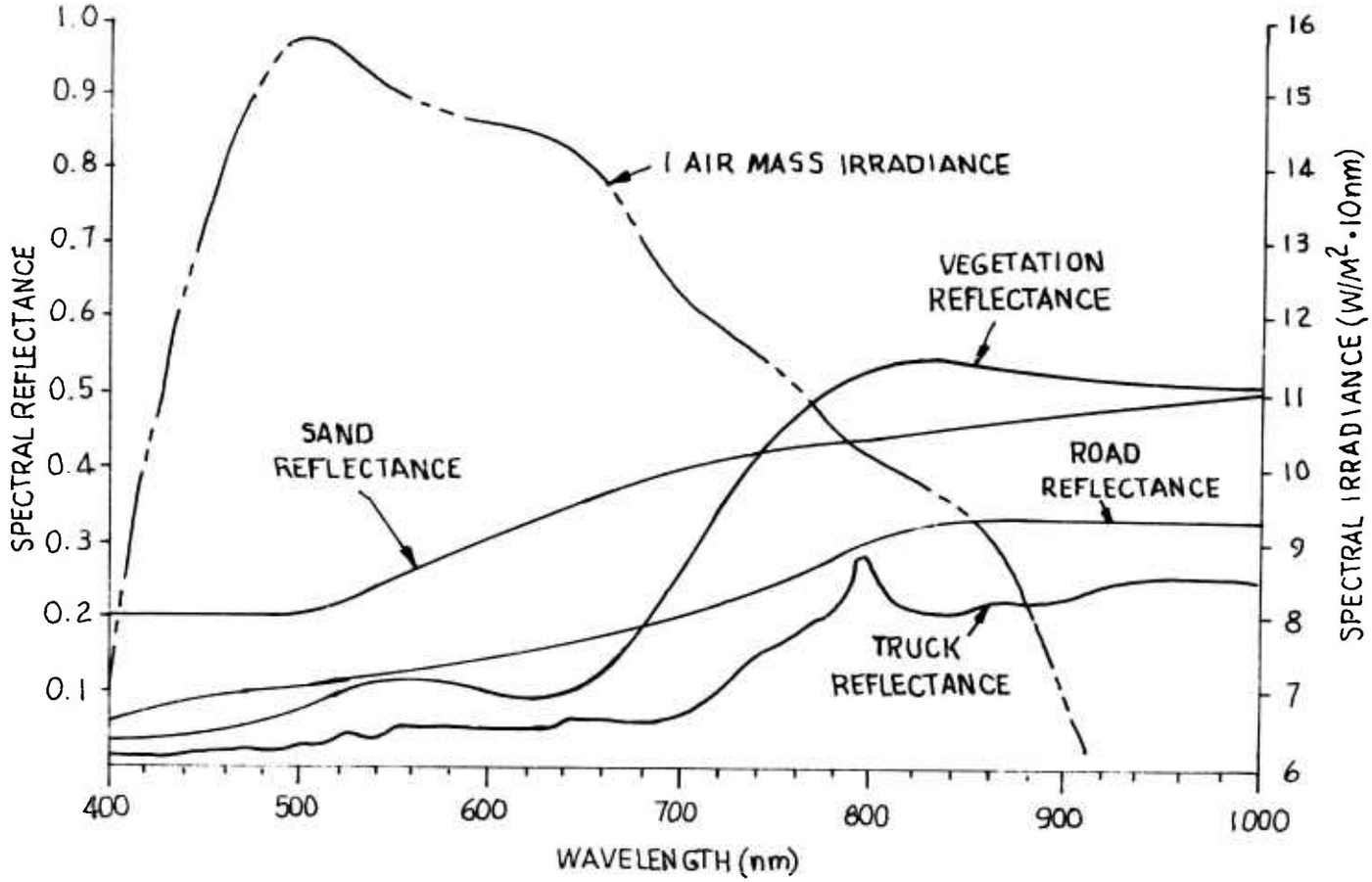


Figure 2-6. Spectral Characteristics

2.3 SENSORS - A1, A2, A3 (SK56079-21-7)

These three assemblies contain the actual Charge Injection Devices mounted in the image planes of the prism beam splitters. The necessary decoupling and biasing networks are located on a board on the back of the CID. (See figure 4-2.)

2.3.1 THEORY OF OPERATION

The CID solid state image sensors use an X-Y addressed array of charge storage capacitors which store photon generated charge in MOS inversion regions. Readout of the first self-scanned arrays was effected by sequentially injecting the stored charge into the substrate and detecting the resultant displacement current to create a video signal. The charge storage sites can be read out in any arbitrary order. Arrays can be designed with integral digital MOS decoders for X and Y line selection to allow "random" access. The integration time as well as the scan sequence could then be externally programmed for special applications.

An array designed for raster scan which includes integral shift registers is diagrammed in figure 2-7 (a). Each sensing site consists of two MOS capacitors with their surface inversion regions coupled such that charge can readily transfer between the two storage regions. A larger voltage is applied to the row connected electrodes so that photon-generated charge collected at each site is stored under the row electrode thereby minimizing the capacitance of the column lines. The sensing site cross-sections, figure 2-7 (b) illustrate the silicon surface potentials and locations of stored charge under various applied voltage conditions.

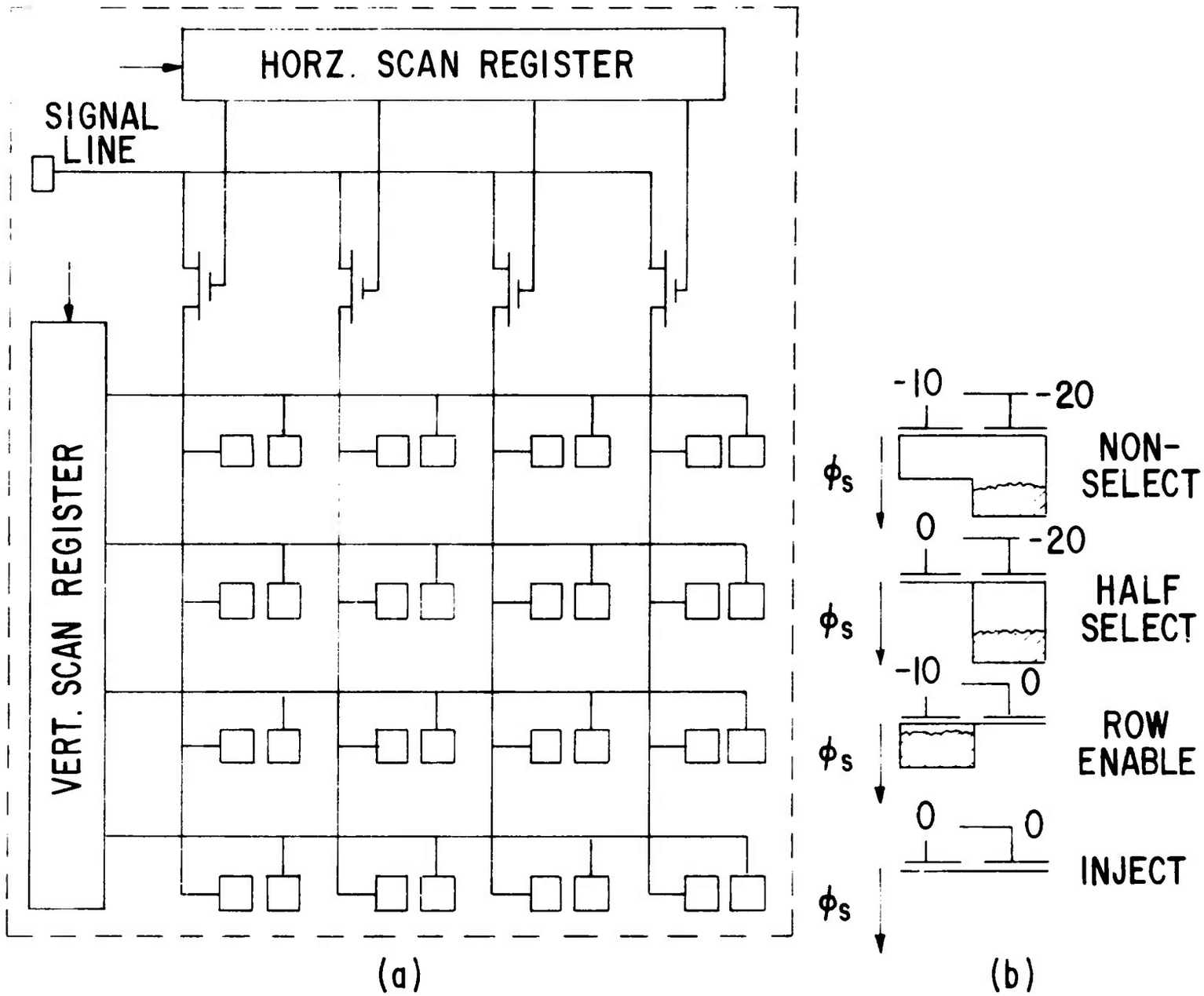


Figure 2-7. Raster Scan CID Array

2.3.1 (Continued)

A line is selected for readout by setting its voltage to zero by means of the vertical scan register. Signal charge at all sites of that line is transferred to the column capacitors, corresponding to the Row Enable condition shown in figure 2-7(b).The charge is then injected by driving each column voltage to zero, in sequence, by means of the horizontal scan register and the signal line. The net injected charge is measured by integrating the displacement current in the signal line, over the injection interval. Charge in the unselected lines remains under the row connected electrodes during the injection pulse time (column voltage pulse). This corresponds to the half select condition of figure 2-7(b). The array is constructed on an epitaxial layer so that the reverse epitaxial junction can act as a collector for the injected charge. This effectively prevents the charge injected at any site from being collected by neighboring sites.

The CID sensors used in the color camera use a new readout technique, termed Parallel Injection, in which the functions and signal charge detection and injection have been separated. The level of signal charge at each sensing site is detected during a line scan and, during the line retrace interval, all charge in the selected line can be injected.

A diagram of 4 x 4 array designed for parallel injection is illustrated in figure 2-8 with the relative silicon surface potentials and signal charge locations included. As before, the voltage applied to the row electrodes is larger than that applied to the column electrodes to prevent the signal charge stored at unaddressed locations from affecting the column lines. At the beginning of a line scan, all rows have voltage applied and the column lines are reset to a reference voltage, V_S, by means of switches S_1 through S_4 and then allowed to float. Voltage is then removed from the line selected for readout (X_3 in figure 2-8) causing the signal charge at all sites of that line to transfer to the column electrodes. Voltage on each floating column line then changes by an amount proportional to the signal charge

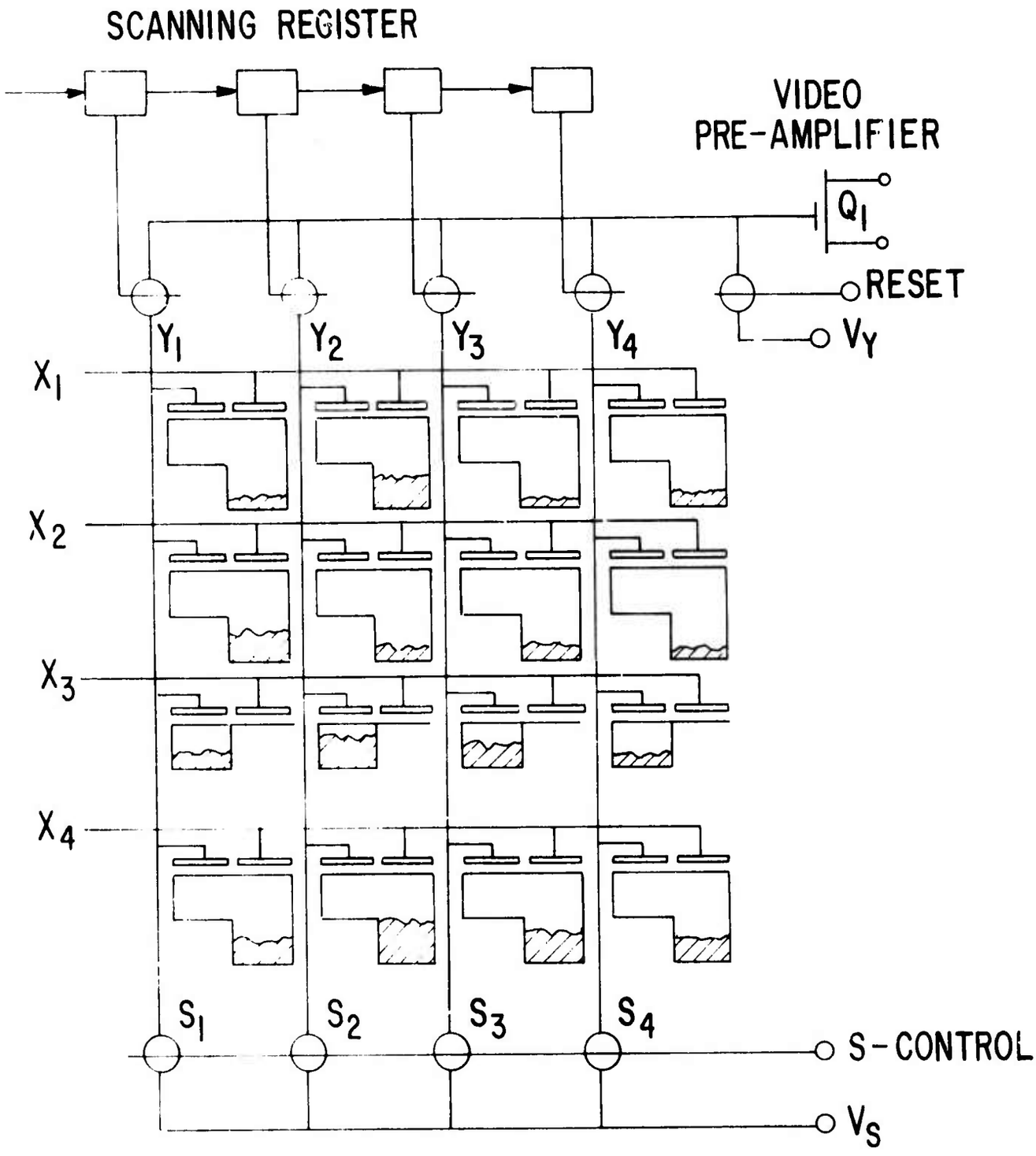


Figure 2-8. Simplified Parallel Injection Configuration

2.3.1 (Continued)

divided by the column capacitance. The horizontal scanning register is then operated to scan all column voltages and deliver the video signal to the on-chip preamplifier, Q_1. The input voltage to Q_1 is reset to a reference level prior to each step of the horizontal scan register.

At the end of each line scan all charge in the selected line can be injected simultaneously by driving all column voltages to zero through switches S_1 and S_4. Alternately, the injection operation can be omitted and voltage reapplied to the row after readout causing the signal charge to transfer back under the row electrodes. This action retains the signal charge and constitutes a nondestructive readout operation.

The actual structure of the 244 x 248 CID used in the color camera employs line and column pairing, and has on-chip preamplifiers as shown in figure 2-9.

The 124 stage horizontal shift register accesses the columns by pairs every 420 nsec. The design of this shift register is such that the outputs driving the column select switches occur during the Ø1H and Ø2H intervals.

The output current waveform contains two interferences. The gate-source capacitance of the reset switches of figure 2-9 couples directly to the output. Similarly, the Ø1H or Ø2H waveform couples to the output. The magnitude of the reset interference is approximately 20 times signal level, with the ØH interference ten times signal level. The method of extracting the video from around the interferences is discussed in the section on the preamplifier.

2.3.2 SUBASSEMBLY INTERFACE

The input-output functions to the CID are listed in Table 2-3 and input/output waveforms shown in figures 2-10 through 2-13.

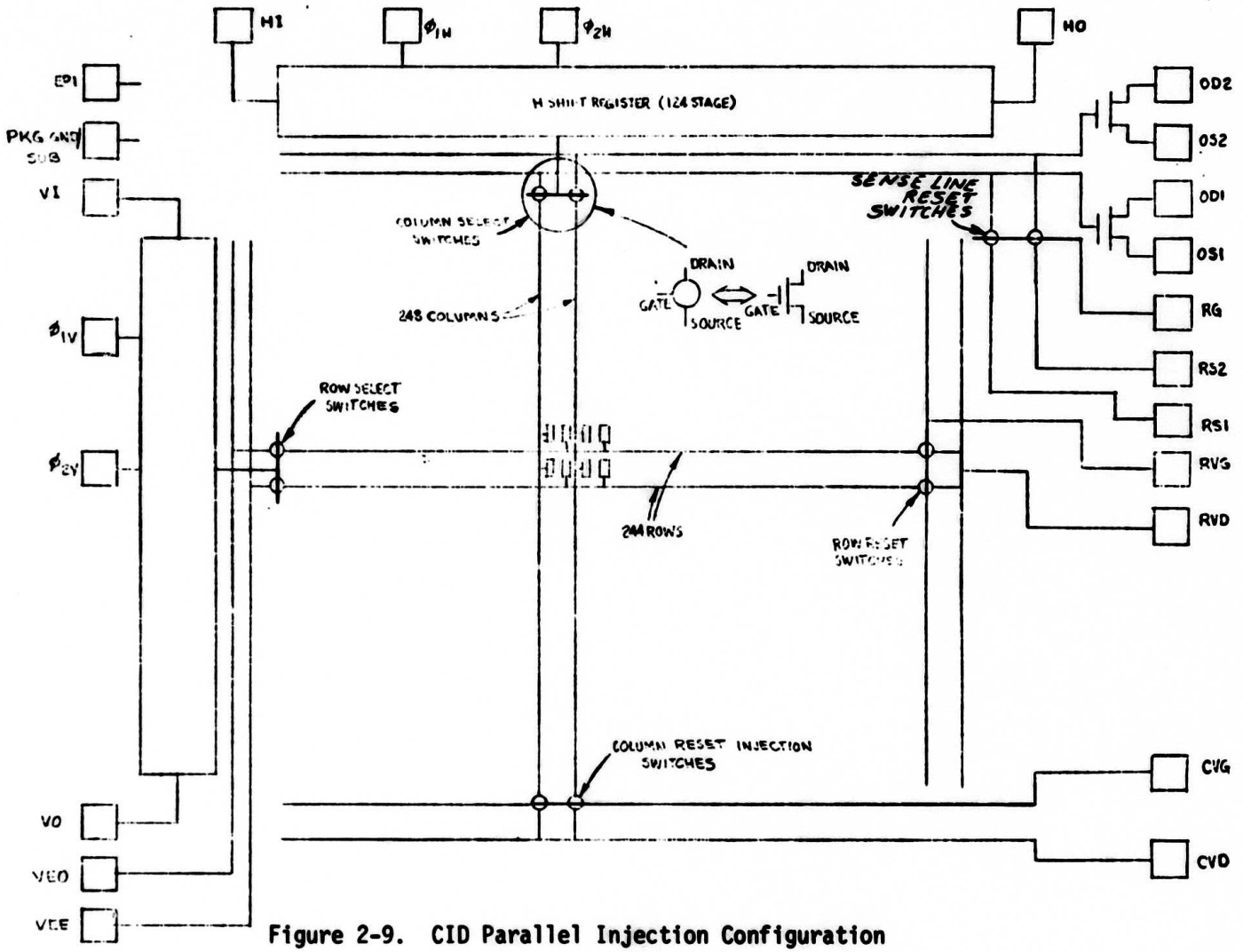


Figure 2-9. CID Parallel Injection Configuration

Table 2-3. CID Camera Interface

FUNCTION	FIG. REF	DESCRIPTION
ϕ_{1H}, ϕ_{2H}	2-10, 2-11	HORIZONTAL PHASE LINES - SELECTS COLUMN PAIR TO BE READ
HI	2-11	HORIZONTAL SHIFT REGISTER INPUT - STARTS HORIZONTAL SCAN
RG	2-10	RESET GATE - DISCHARGES SENSE LINE CAPACITANCE PRIOR TO READING AN ELEMENT PAIR
RS1, RS2		RESET SOURCE 1 AND 2 - ESTABLISHES REFERENCE VOLTAGE V_R ON THE SENSE LINE, WITH $-8V \geq U_R \geq -10V$. NOISE ON THIS LINE IS COUPLED 1:1 INTO THE SENSE LINE. DIFFERENCE BETWEEN RS1 AND RS2 ESTABLISHES EVEN / ODD PATTERNING
ϕ_{1V}, ϕ_{2V}	2-12, 2-13	VERTICAL PHASE LINES - SELECTS ROW PAIR TO BE READ
VI	2-13	VERTICAL INPUT - STARTS VERTICAL SCAN
VEO	2-12, 2-13	VERTICAL ENABLE - ODD
VEE	2-12, 2-13	VERTICAL ENABLE - EVEN - SELECTS ROW TO BE READ FROM THE PAIR SELECTED BY THE VERTICAL SHIFT REGISTER.
CVG	2-12, 2-13	COLUMN GATE - CAUSES ALL COLUMNS TO BE SIMULTANEOUSLY CONNECTED TO CVD TO INJECT LINE JUST READ AND INITIALIZE COLUMNS PRIOR TO ROWSCAN.
CVD	2-12, 2-13	COLUMN DRAIN VOLTAGE - CAUSES INJECTION OF THE COMPLETE ROW JUST READ. NOISE ON THIS LINE IS COUPLED 1:1 INTO THE SENSE LINE. DIFFERENCE BETWEEN VOLTAGE AT CVD (AT END OF CVG) AND RS1 OR RS2 ESTABLISHES BLACK LEVEL
RVG	2-12, 2-13	ROW GATE VOLTAGE - ASSISTS RESET OF LAST ROW READ AND MAINTAINS BIAS ON ROWS.
RVD		ROW DRAIN - BIAS VOLTAGE (-20V TO -18V) ON ROW DURING INTEGRATION PERIOD (i.e. WHEN NOT BEING READ)
OS2		PRE AMP SOURCE EVEN
OD2	2-10	PRE AMP DRAIN EVEN
OS1		PRE AMP SOURCE ODD
OD1	2-10	PRE AMP DRAIN ODD - OUTPUT FET HAS g_{fs} = 2 mmho AT 3 MA AND 1.5 mmho AT 2MA NOMINAL.
EPI		EPITAXIAL BIAS - OPERATED AT 0 VOLTS
SUB (PACKAGE CID)	2-12	SUBSTRATE - BIASED TO CANCEL PARABOLIC SHADING COMPONENT OF OUTPUT VIDEO.

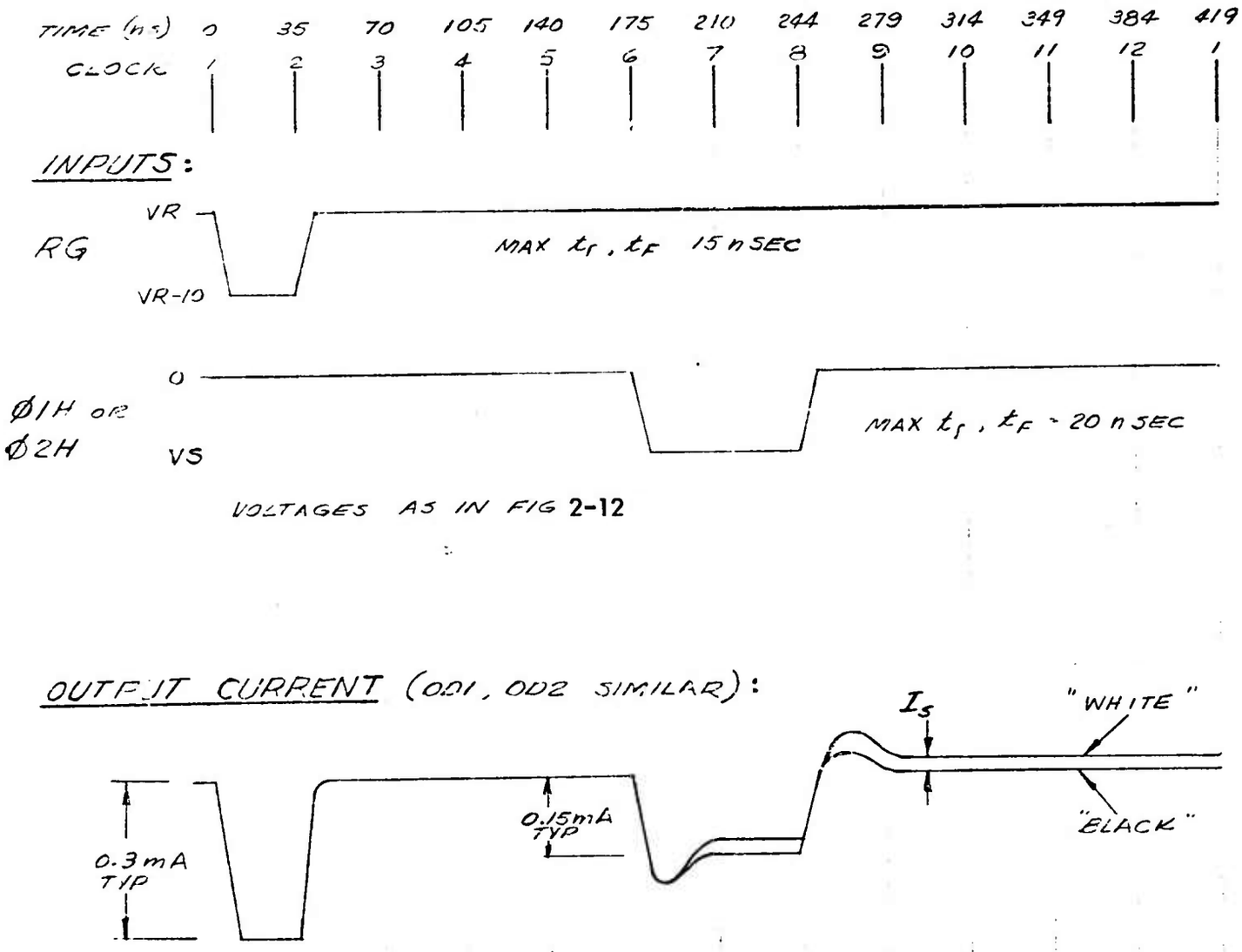


Figure 2-10. Element Rate Timing

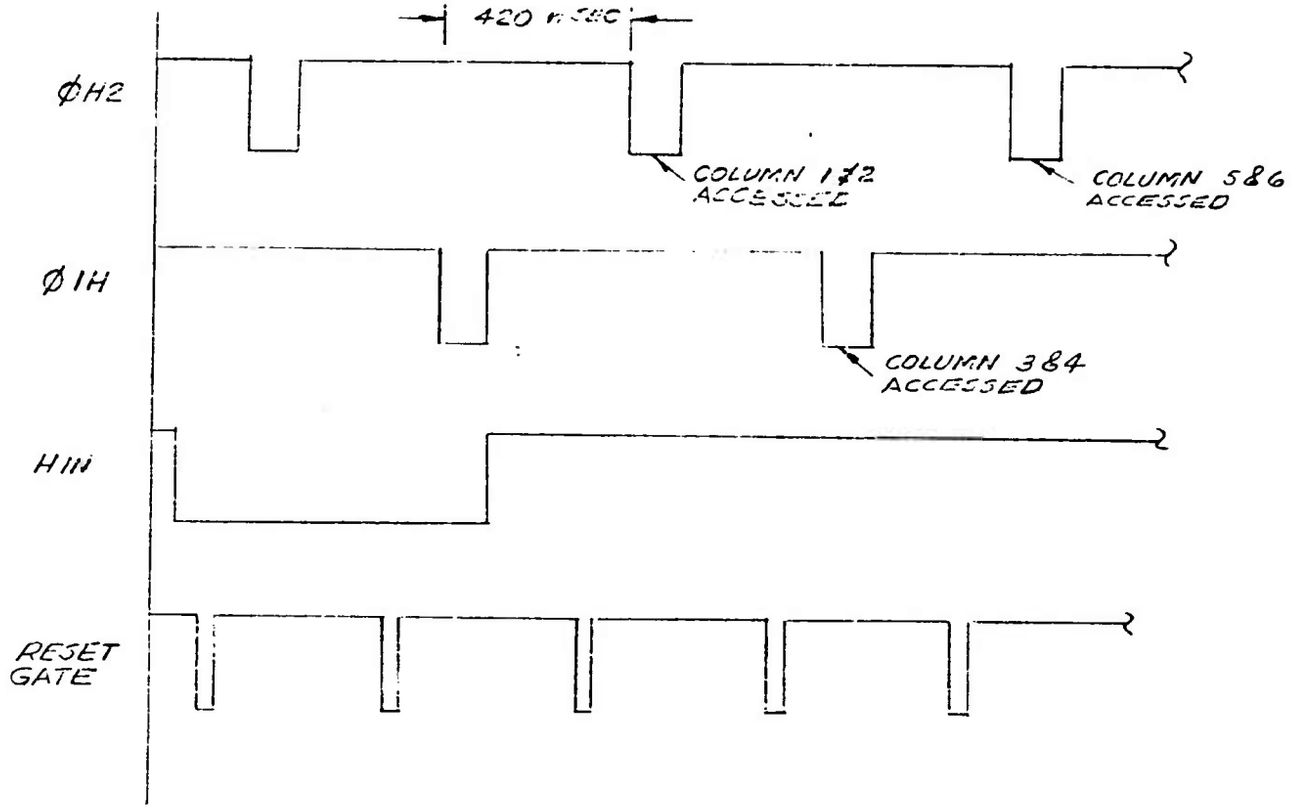


Figure 2-11. Horizontal Input and Phase Line Timing

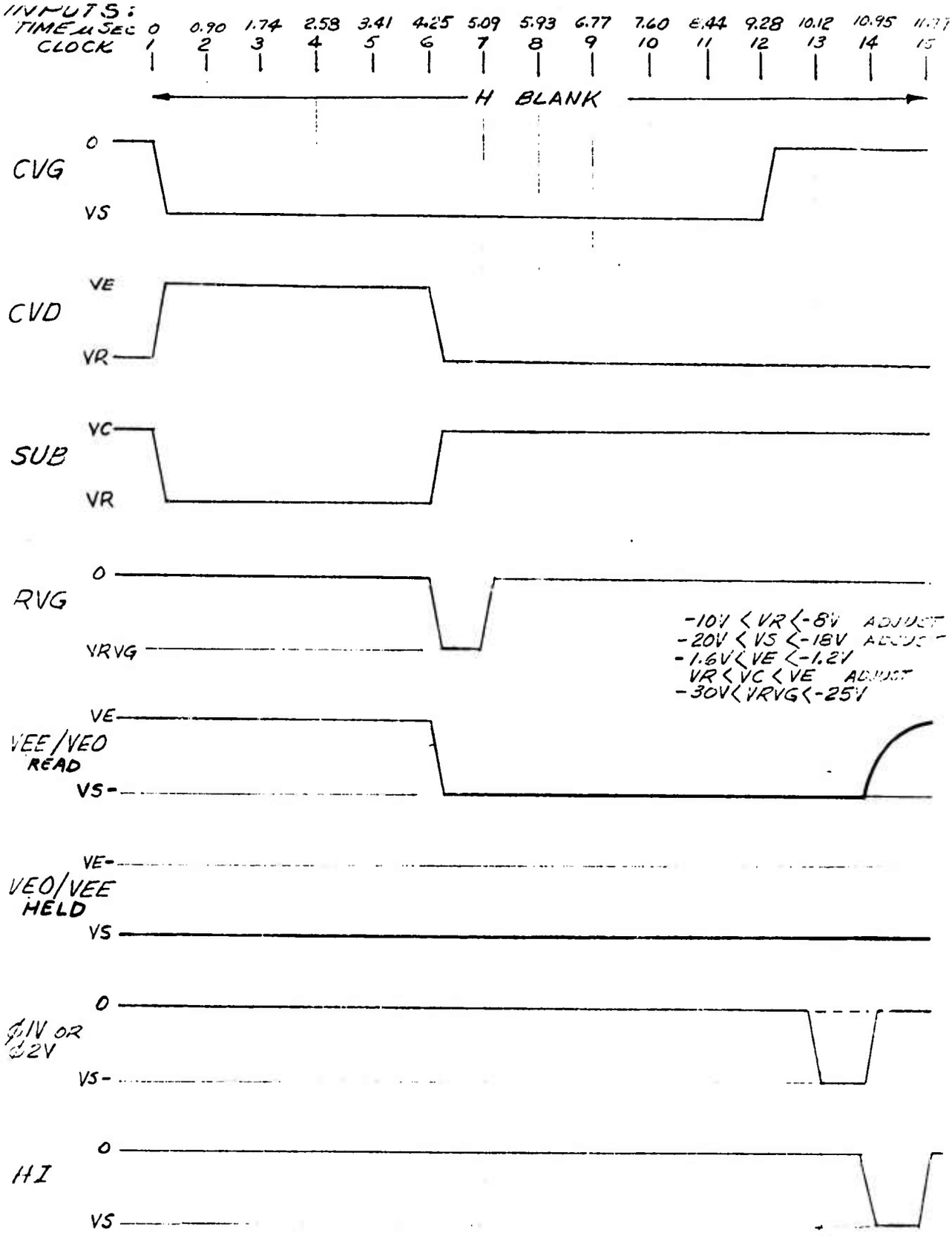


Figure 2-12. Line Reset Injection Timing

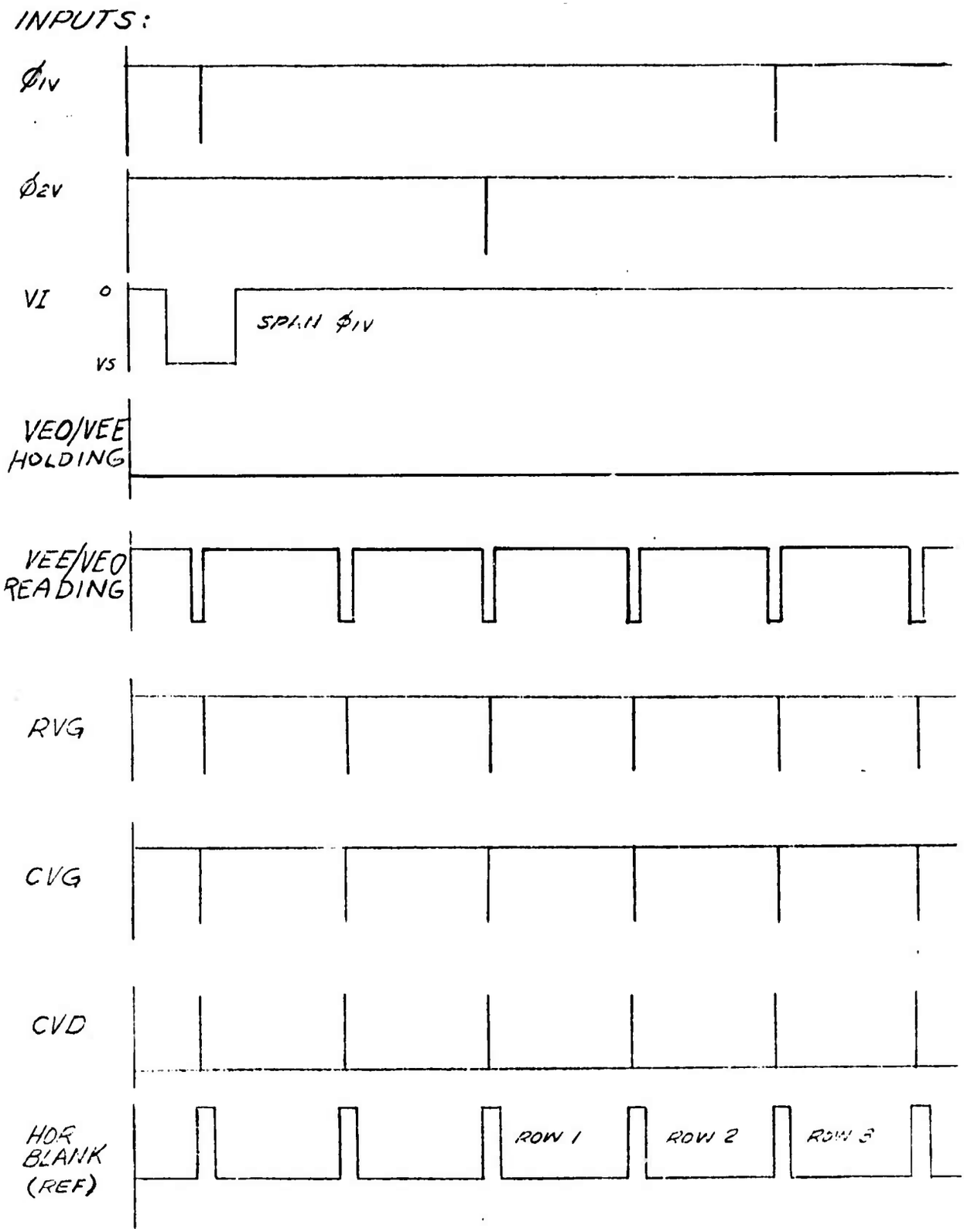


Figure 2-13. Line Rate Timing (Start of Readout)

2.4 DRIVER A4, AND OSCILLATOR A5 (SK56079-21-8)

The Driver board provides the eleven MOS level drive signals to each of the three CID's, along with their required DC biases. In ddition, the synchronizing signals necessary for the operation of the preamplifier and other camera electronics are provided. The oscillator (A5) is a purchased subassembly, and is mounted on a board separate from the Drivers. (See figure 4-2.)

2.4.1 SUBASSEMBLY INTERFACE

Outputs:

TO CID

Specified in paragraph 2.3.2

TO PREAMPLIFIER (TTL LEVELS)

MUX
$\overline{\text{MUX}}$
SAMPLE
RESTORE
ØCOR

} SK56079-21-26 (See figure 4-4.)

TO CANCELER, PROCESSOR, ENCODER (TTL LEVELS)

30 Hz	- squarewave, referenced to field
H/2	- squarewave, toggles in H blank
KC	- (key clamp); in H Blank
VITS 17	- logical 1 in line 17 each field
PILOT CLOCK	- 2 MHz squarewave in VITS 17
$\overline{\text{ECB}}$	- (extended composite blank) RS170 composite blank with horizontal component extended 0.5 µsec
$\overline{\text{CS}}$	- (composite sync)
$\overline{\text{BF}}$	- (Burst flag)
14 MHz	- 14.31818 MHz squarewave

} RS170 timing

2.4.2 THEORY OF OPERATION

The block diagram of the driver scan logic is shown in figure 2-14. The oscillator is mounted on a separate assembly. The basic clock rate of 14.31818 MHz $\pm$ 40 Hz, when divided by four, gives the standard color subcarrier frequency of 3.579545 MHz $\pm$ 10 Hz. The oscillator is temperature compensated to remain within tolerance over a range of -20°C to +70°C.

This same clock, when effectively divided by 3, gives the element rate of 4.77 MHz, which fits the 248 horizontal elements into 51.96 µsec which is approximately the horizontal active time.

The sync generator as shown in figure 2-14 consists of a divide-by-seven counter U1 to provide 2.04545 MHz to the monolithic sync generator U3. This circuit has as output the standard television timing signals of composite sync, composite blanking, horizontal and vertical drives, and burst flag in accordance with EIA standard RS-170. The horizontal component of composite blanking is extended by approximately 0.5 µsec to match the active time of the sensor. The blanking signal is thus denoted as ECB for extended composite blank.

The sync generator portion of the scan logic derives two reset signals, $\overline{HC}$ (Horizontal Clear) and VRT (Vertical Reset). $\overline{HC}$ resets the element scan logic to restart in the same state each line, and resets the injection logic to initiate the injection cycle. U2a is used to derive $\overline{HC}$ and U2B derive VRT.

The element scan logic is clocked by the 14 MHz clock and reset each line by $\overline{HC}$. The basic timing is established by a six-bit Johnson counter with split clock.

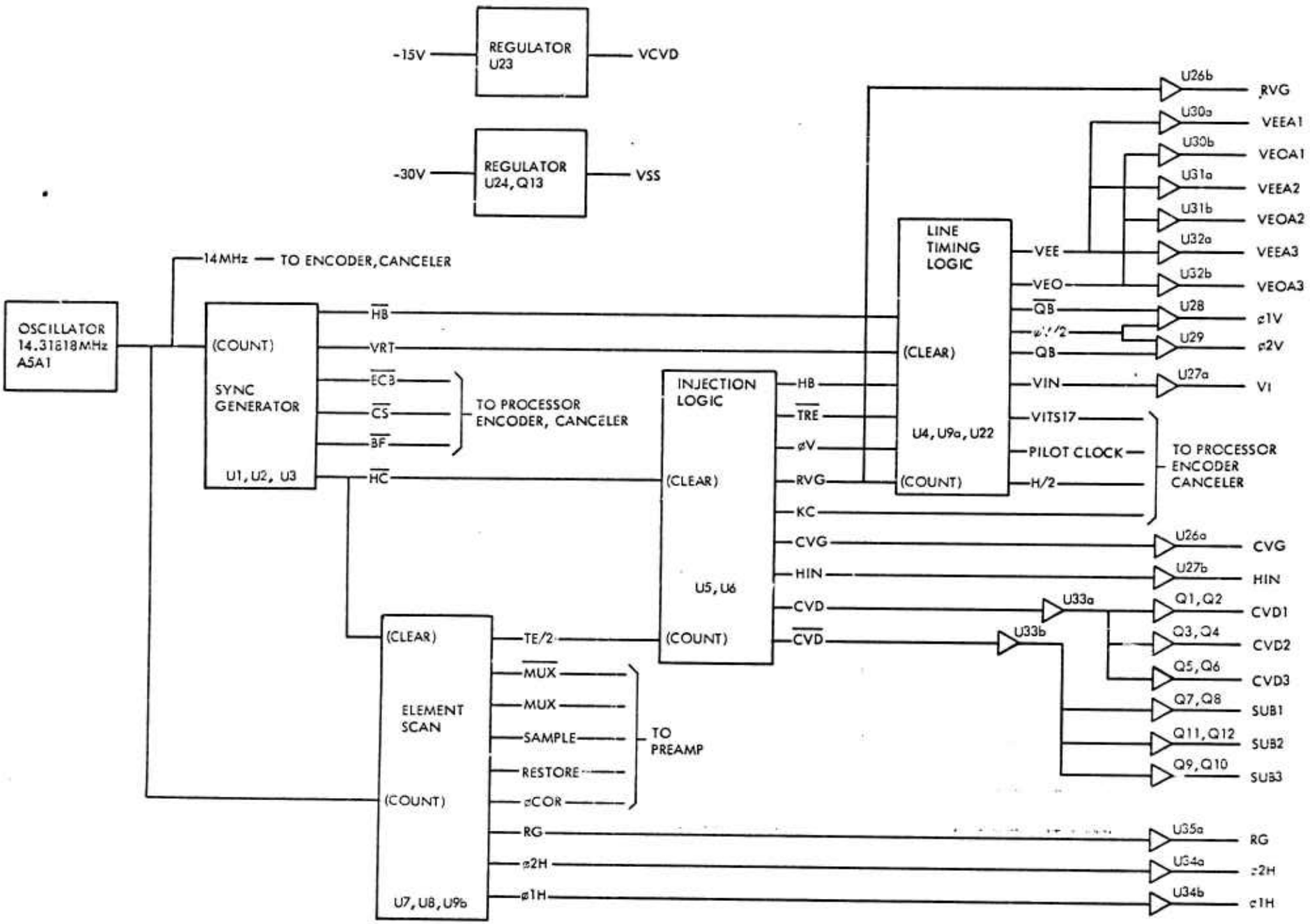


Figure 2-14. Driver A4 Block Diagram

2.4.2 (Continued)

This is basically a six stage shift register with its output complemented and fed back into its input. This results in the waveforms shown in figure 2-15. Initially the counter is cleared. For the first six clocks, a logical 1 is shifted into the register. For the next six clocks,a logical 0 is shifted in. Thus in 12 clocks, the counter has gone from cleared back to being cleared, and the cycle repeats. The even numbered stages are clocked by CK, and the odd stages are clocked by $\overline{CK}$. Since CK is a squarewave, this gives a 35 μsec interval between the effective clock times of the counter which is the time resolution of a 28 MHz clock.

The element rate signals may be decoded simply from the counter outputs in a single 2 input AND or NAND gate. For example, to obtain a pulse between clock #3 and #5, the signals at WT34 and WT42 may be ANDed together. For output pulses up to 6 clocks long, an AND gate may be used. For pulses longer than 6, a NAND gate will give a positive pulse.

The virtue of the Johnson counter in this application is its ability to simply decode various pulse lengths with different positions in the cycle by changing two inputs to the decoding gates. In addition, since only one flip-flop changes state on each clock, there are no "glitches" due to any race conditions.

The actual interconnection of the decoder inputs with the Johnson counter outputs is detailed in Drawing SK56079-21-26 (figure 4-4).

The injection logic is also based on a Johnson counter, but with 8 bits clocked together. The clock is provided by the ÷ 2 used to separate even and odd clocks to the horizontal shift register. The final state of the counter is decoded by U15D and used to gate off the clock. Thus, the counter is cleared by $\overline{HC}$ at the beginning of horizontal blanking, and counts for 15 clocks and stops until the next $\overline{HC}$. Since the clock rate is approximately 0.8 μsec, and the counter runs for 15 counts, the counter runs through a single cycle of 12 μsec.

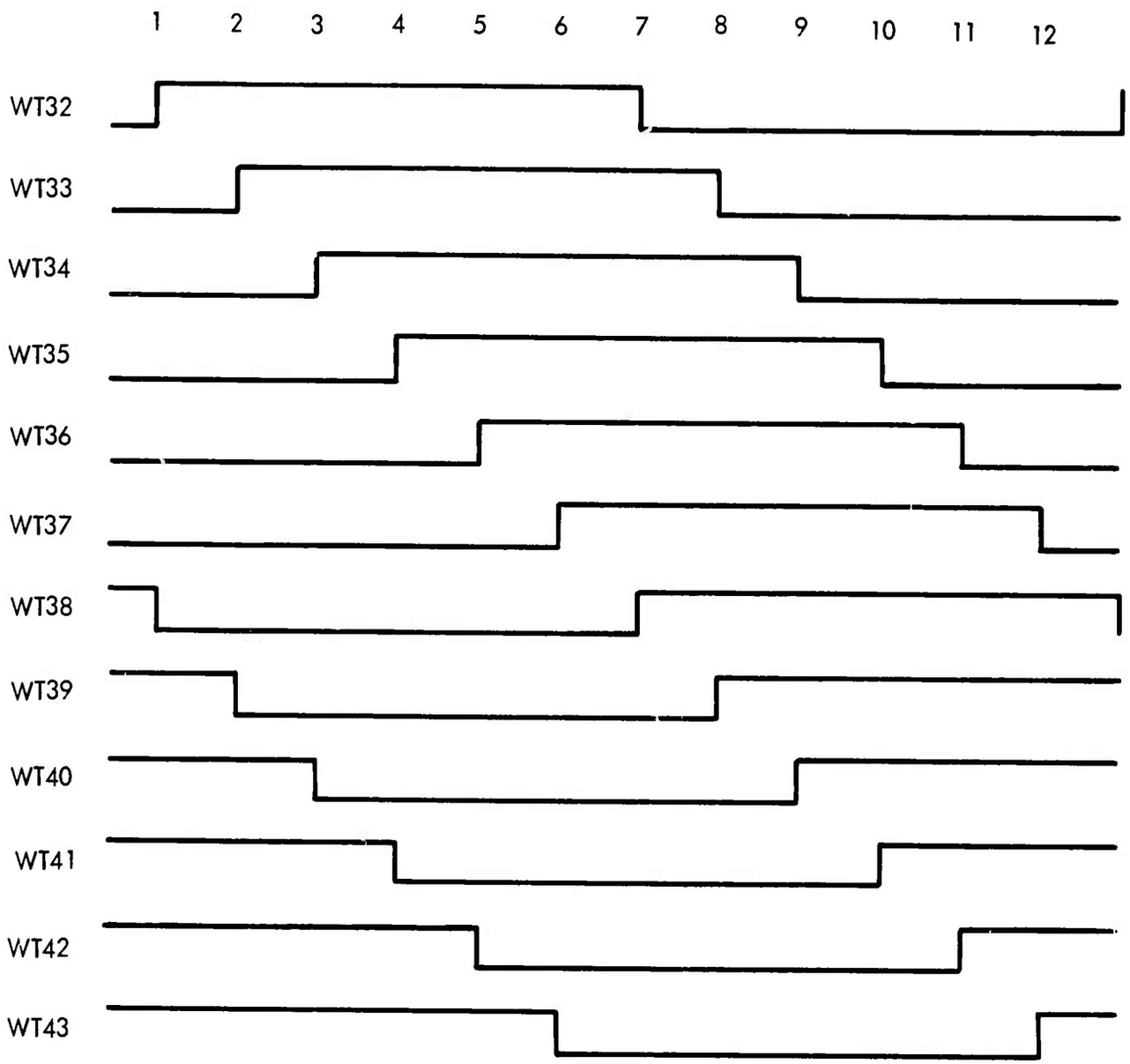


Figure 2-15. Element Scan Time Base

2.4.2 (Continued)

As with the element scan logic, the outputs are decoded with single 2 input gates, as detailed in SK 56079-21-26 (figure 4-4).

The last segment of the logic is the Line Timing Logic of figure 2-14. This derives those signals which occur on a line to time basis.(such as VEE, VEO, Ø1V, Ø2V), or occur once during vertical retrace (such as VIN, VITS17 and PILOT CLOCK). The lines are counted by U4. After the last output in vertical blanking, U9A is toggled to prevent the V rate signals from reoccuring.

The 30 Hz frame rate squarewave is derived by U22. The first flip-flop U22a toggles on burst flag. Due to the 2:1 interlaced sync format, there are an even number of BF on one field, and an odd number on the next. Thus at the vertical reset, VRT, the state of U22a is determined by the field.

There are 21 drivers of various types to provide the drive to the sensors. They are all purchased hybrid devices with the exception of the CVD and SUB drivers, which are discrete CMOS.

The drive levels are set by the two voltages VCVD, which is approximately -10V, and VSS, which is approximately -20V. The reset source biases RS1 and RS2 to the CID are derived by U25 from VCVD. Each sensor has two adjustments, the difference between RS1 and RS2, (set by R16, R18, and R19) and the difference between the average of RS1 and RS2 and VCVD (set by R15, R17, and R19). The first voltage shows up as even/odd column interference in the video, and the second group of adjustments set the level during blanking out of the preamplifier. Both of these must be adjusted to compensate for parasitic capacitances in the CIDs themselves.

The vertical enable outputs VEE and VEO for each sensor may be adjusted by R47, R50, and R53 to eliminate even/odd line to line pairing.

The substrate drive levels set by R55, R56, and R57 must be adjusted to give minimum peak-peak shading in the video out of the preamplifiers.

2.5 PREAMPLIFIER A6 (SK56079-21-10)

The preamplifier extracts the video information from the CID by double sampling the output waveforms from each CID, and multiplexing the two parallel channels from each sensor into a single video output. The double sampling is used to effectively eliminate 1/f noise from the on-chip preamplifier of the CID. The preamplifier assembly contains three identical circuits, one for each sensor. (See figure 4-3.)

2.5.1 SUBASSEMBLY INTERFACE

Inputs:

OD1A1
OD2A1
OD1A2
OD2A2
OD1A3
OD2A3
} Output Drain, Even and Odd, from each sensor

SAMPLE - TTL, figure 2-16

RESTORE - TTL, figure 2-16

ØCOR - TTL, Alternate element pairs

Outputs:

SENSOR 1 VIDEO
SENSOR 2 VIDEO
SENSOR 3 VIDEO
} 0.2 vpp, Black Negative

2.5.2 THEORY OF OPERATION

The block diagram of one of the three identical channels of the preamplifier is shown in figure 2-17. The components indicated are for the sensor 1 channel, but the discussion applies equally to all three channels.

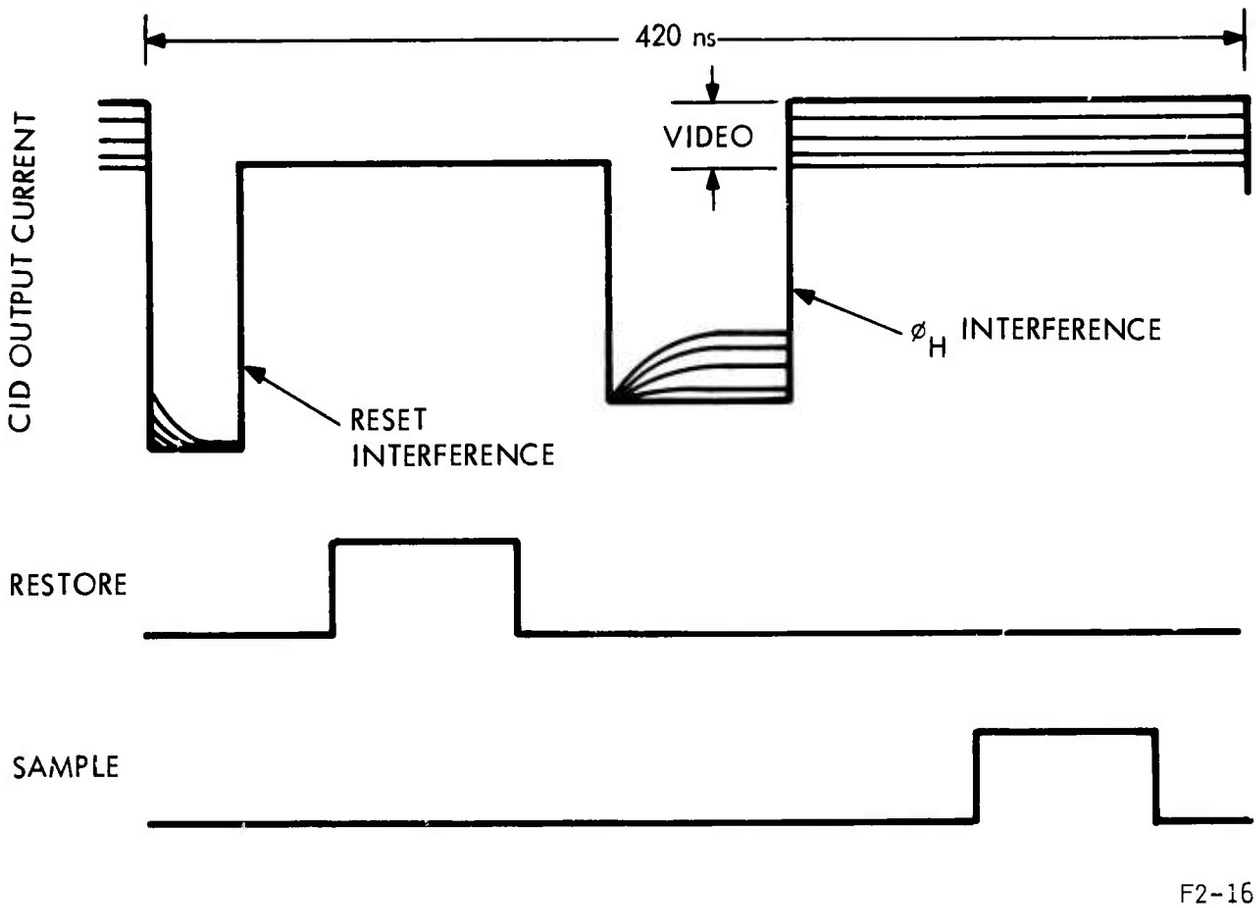


Figure 2-16. Preamplifier Input Timing

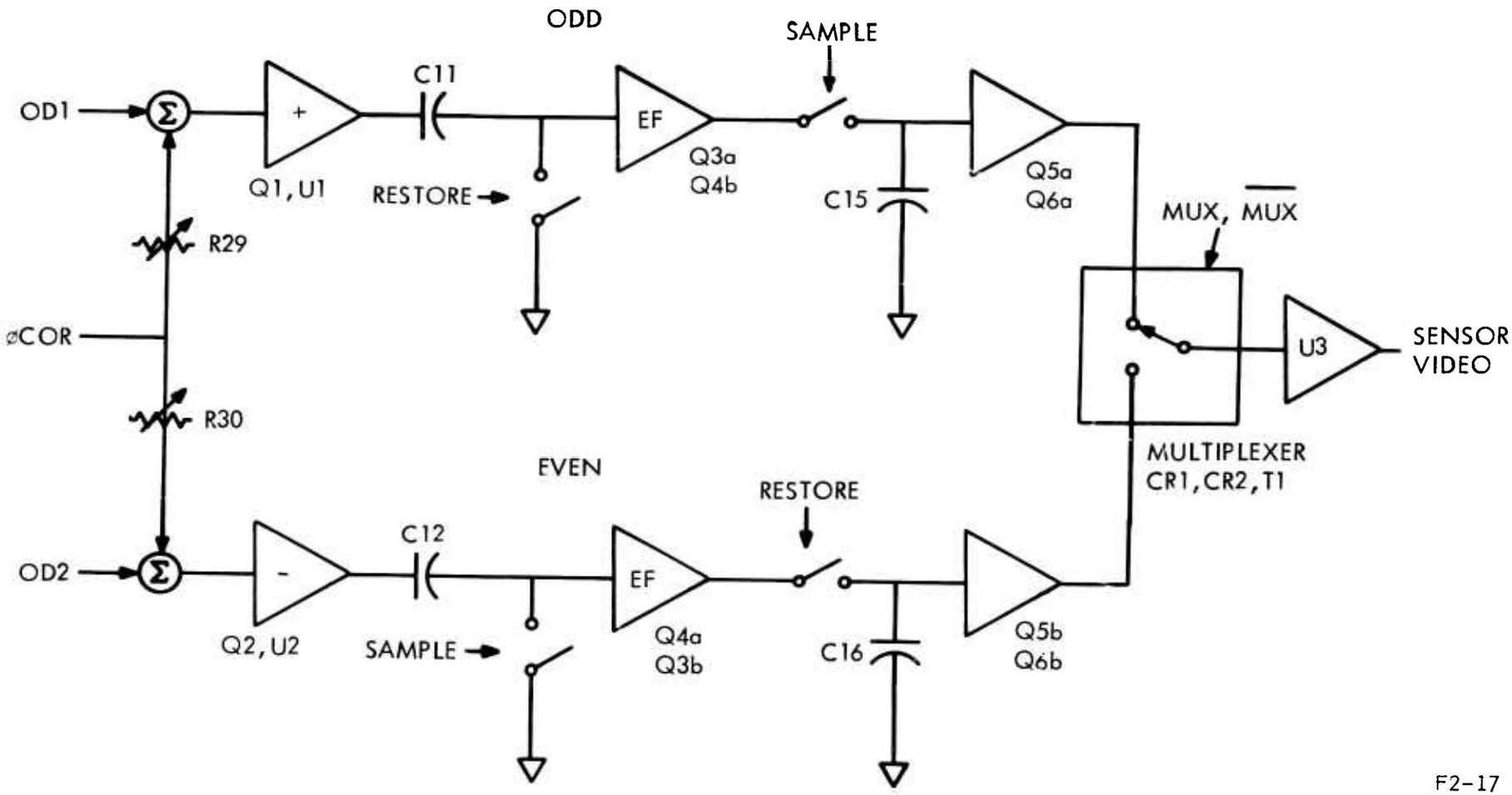


Figure 2-17. Preamplifier, Single Channel Block Diagram

2.5.2 (Continued)

The even and odd outputs from a CID are similar, and are treated similarly, but not identically, in the preamplifier. The pair of sites are accessed simultaneously every 420 nsec. In order to display the sites in proper order, the even element must be delayed by 210 nsec. This is achieved by appropriate timing changes in the double sampler to be discussed later.

The two input currents of figure 2-16 are passed through cascode stages Q1 and Q2, and amplified to a video level of approximately 0.2 vpp, with the reset and ØH interference clipping. Both waveforms are then double sampled to remove the interferences from the video.

The basic double sampler as shown in figure 2-18 consists of a series sample and hold S1 and C1, a unity gain buffer, and a conventional sample and hold, S2 and C2, with its unity gain buffer.

The series sampler S1, C1 is identical to a conventional DC restorer. It effectively subtracts the sampled voltage from the input signal. This waveform is sampled a second time giving as output the difference between the input voltage when S2 is closed and when S1 is closed.

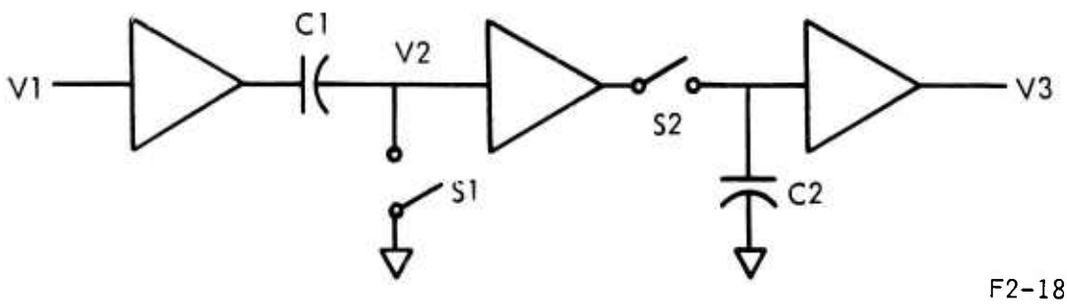


Figure 2-18. Double Sampler

2.5.2 (Continued)

The sampling occurs in the two intervals shown in Figure 2-16. During the RESTORE interval the waveform has a reference level, and in the SAMPLE interval it has video. The desired video information, then, is the difference between these levels. As shown in Figure 2-17, the odd channel takes the first sample during RESTORE and the second sample during SAMPLE.

The even channel has the SAMPLE and RESTORE functions reversed, i.e., the first sample occurs in the SAMPLE interval, and the second in the RESTORE interval. This introduces the delay of roughly 210 nsec which is necessary to offset the even columns in the video output. Even and odd video are double sampled and multiplexed to the output as shown in figure 2-17.

The timing may be seen in Figure 2-19, where both odd and even channels over two element pairs is shown. The odd and even inputs are essentially identical in form, with different video levels shown. Elements 3 and 4 are read simultaneously. The odd sampled video for element 3 appears after SAMPLE, and contains interference coincident with SAMPLE. The element 3 level is held for 350 nsec until the next SAMPLE. The even video appears on the holding capacitor with RESTORE, approximately 175 nsec after the even video, and containing RESTORE interference.

The multiplexer switches the output between even and odd sampled video every 210 nsec. MUX must be positioned to avoid passing the SAMPLE or RESTORE interference to the video. Then the only interference which will be in the output video will be due to the multiplexer itself.

This method of delaying the even channel inverts the sampled video. This is corrected by having a negative gain in the amplifier prior to the sampler string.

2.5.2 (Continued)

In the CID, the Ø and Ø2H are coupled differently into the output. This shows up in the picture as a brighter or darker column every four elements. This may be approximately canceled by summing an adjustable amount of ØCOR independently into the even and odd channels through R29 and R30.

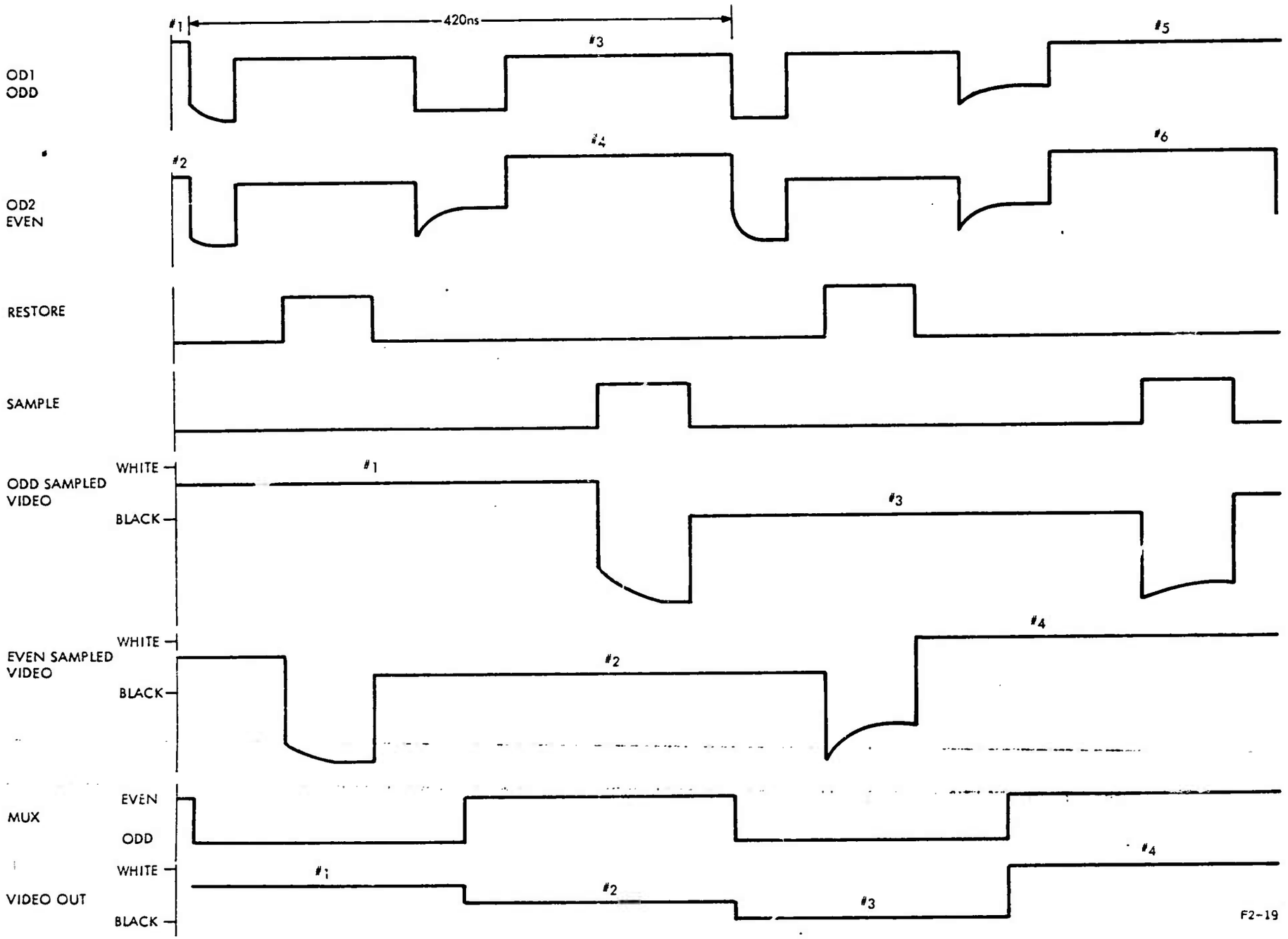


Figure 2-19. Preamplifier Sampler and Multiplexer Timing

2.6 FPN CANCELER A9 (SK56079-21-13)

The fixed pattern noise canceler reduces the column interference and the horizontal shading from the CID sensor and properly formats the video for display for each of the three sensor channels. In addition, field flicker correction is provided, along with blanking, black and white clip. (See figure 4-6)

2.6.1 SUBASSEMBLY INTERFACE

Inputs:

Video:

Sensor 1 video
Sensor 2 video
Sensor 3 video
} 0.2 vpp into 75 ohms

TTL (positive true)

H/2 squarewave
30 Hz squarewave
14 MHz squarewave
KC (k · clamp) logical 1 within horizontal blanking
ECB: logical 0 during blanking

Outputs:

Video 1
Video 2
Video 3
} 0.2 vpp into 75 ohms

2.6.2 THEORY OF OPERATION

A simplified block diagram of one channel of the FPN Canceler is shown in Figure 2-20. The three channels are identical with common drive and timing circuits.

The vertical timing of the CID imager is such that the 122 odd numbered rows of the CID array are read out during the active (unblanked) portion of one field. Each row is read twice in succession to provide a match to the 244 lines required for one field of a 2:1 interlaced picture. The even numbered rows of the array are read in a similar fashion during the next field.

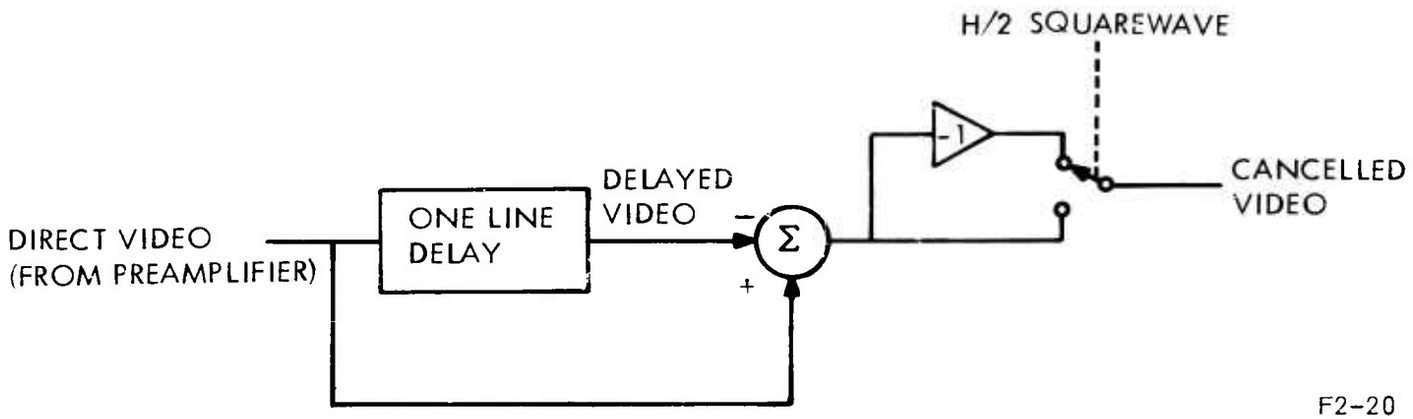


Figure 2-20. Single Channel of FPN Canceler, Simplified Block Diagram

2.6.2 (Continued)

The first reading of any row provides the video information plus the fixed pattern noise on that row, and discharges the stored signal charge. The second reading of the row thus contains no video information, but the same fixed pattern noise associated with the scanning process will appear at the input to the canceler.

As shown in Figure 2-20, in the canceler, the direct video is delayed by one horizontal line time (63.56 usec) and subtracted from undelayed video. Every other line is inverted to give canceled video. For the odd field, this gives the sequence shown in Table 2-4, where r_n denote the video information on CID row n, and f_n denotes the fixed pattern noise on row n.

If the linearity and frequency response of the direct and delayed channels are matched, then every other video line will contain only video and will have the fixed pattern noise canceled completely. The remaining lines contain the difference between the noise on two different rows. The effectiveness of the cancellation depends on how well the noise matches.

The even field operation is identical with the exception that the even lines are read giving the display sequence row 2, 2, 4, 4, 6, 6, etc.

The two fields are interlaced on the display giving the line format of Table 2-5. The lines are not in the proper sequence. This tends to reduce vertical resolution and produces a jog in a diagonal line every four display lines.

Table 2-4. Odd Field Sequence, FPN Canceler

DIRECT	DELAYED	DIFFERENCE	POLARITY	VIDEO	NOISE
V_1+f_1	0	V_1+f_1	+	V_1	f_1
f_1	V_1+f_1	$-V$	-	V_1	0
V_3+f_3	f_1	$V_3+(f_3-f_1)$	+	V_3	(f_3-f_1)
f_3	V_3+f_3	$-V_3$	-	V_3	0
V_5+f_5	f_3	$V_5+(f_5-f_3)$	+	V_5	(f_5-f_3)
f_5	V_5+f_5	$-V_5$	-	V_5	0
V_7+f_7	f_5	$V_7+(f_7-f_5)$	+	V_7	(f_7-f_5)
f_7	V_7+f_7	$-V_7$	-	V_7	0

Table 2-5. Line Format for Interlaced Display

INTERLACED DISPLAY:

FIELD	DISPLAY LINE	CID ROW
ODD	1	1
EVEN	1	2
ODD	2	1
EVEN	2	2
ODD	3	3
EVEN	3	4
ODD	4	3
EVEN	4	4
ODD	5	5
EVEN	5	6
ODD	6	5
EVEN	6	6
ODD	7	7
EVEN	7	8
ODD	8	7
EVEN	8	8

2.6.3 CIRCUIT DESCRIPTION

A more complete block diagram of the FPN Canceler is shown in Figure 2-21. The input video is passed through a low pass filter which cuts off at 3 MHz to restrict the sampling transients from the preamplifier. The 1H delay uses a quartz delay line with an IF bandpass of 4 to 8 MHz. The video to be delayed uses a vestigial sideband, suppressed carrier AM with a carrier frequency of 7.16 MHz. This gives a 3 MHz bandpass on the lower sideband, with the upper sideband suppressed above 0.8 MHz.

The video is modulated by the balanced modulator U1. The network R9, R10, and C4 provides correction for the suppressed upper sideband. The output of U1 is filtered by the doubly resonant circuit L1, C5, L2. This peaks the response of the delay line at the outer limits of its bandpass to give a flatter frequency response over the passband.

U2 drives the high capacitance of the quartz delay line DL1. The output of the delay line is demodulated by the balanced demodulator U3 to give baseband video. The overall frequency response through the delayed channel is approximately 2.5 MHz (3 dB) which is compatible with the 2.38 MHz Nyquist limit of the CID array.

The delay through DL1 is 63556 ns which is equal to the TV line time in a color system. There is approximately 20 ns additional delay through the electronics of the delay channel which is compensated by the distributed constant delay line DL1 in the direct channel. The high frequency response is trimmed by C5 to match the delayed channel.

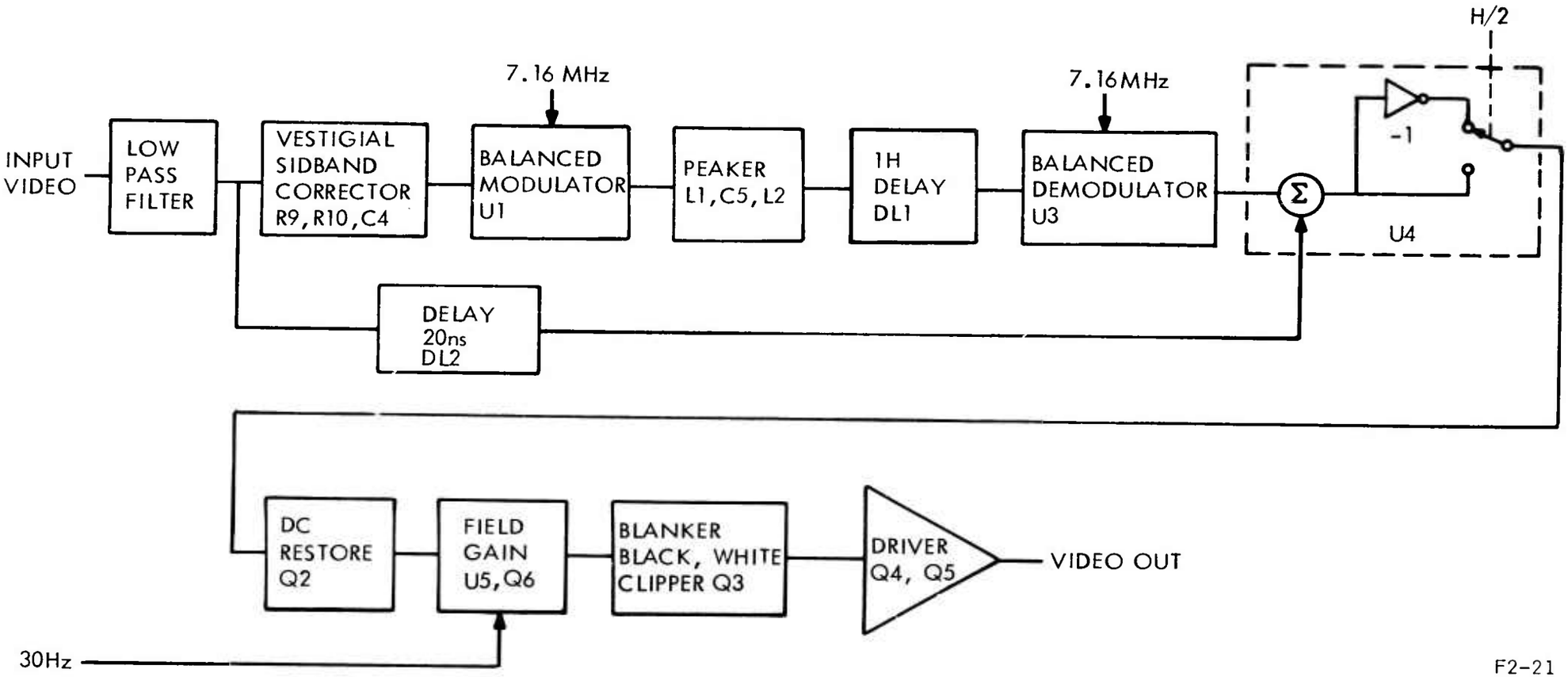


Figure 2-21. Single Change of FPN Canceler, Detailed Block Diagram

2.6.3 (Continued)

The differencing and inversion is done by a single device U4, which is a video switch with two differential inputs. A TTL drive switches between the two inputs each line. One input is connected for direct minus delayed and the other input is delayed minus direct. The output of U4 is thus cancelled video.

The cancelled video is dc restored by Q2 and amplified by U5. Q3, CR1 and CR2 provide blanking, white, and black clip. Q4 and Q5 buffer the output to drive a 75 ohm load.

One CID fault is emphasized by this readout technique. If there are mask alignment errors in the manufacture of the array, even and odd rows may have different sensitivities. Since they are displayed on alternate fields separated by 1/60 sec, this difference in even/odd field gain will appear as a flicker in whites. The problem is alleviated by changing the gain of U5 on a field basis by switching Q6 on in the feedback network of U5, in either the even or odd field as required. Proper phase is selected by connecting C26 to either pin 10 or 11 of U17. Then R39 may be adjusted to null flicker. This is not completely successful in eliminating field flicker, since for some mask misalignments the sensitivity will vary with position in the array.

2.7 COLOR PROCESSOR A7 (SK56079-21-11)

The color processor provides a matched automatic gain control (AGC) on the three video channels from the imager, and matrixes these into red, green, and blue video for ultimate display on a color monitor. The gains of the three channels are matched in order to maintain color balance as the AGC adjusts through its 40 dB range. There are two remotely selectable plug-in matrices which may have either positive or negative coefficients.

2.7.1 SUBASSEMBLY INTERFACE

Inputs

Video - Video 1, Video 2, Video 3 — 0.2V pp black negative, blanked

TTL Levels (positive true)

VITS 17 : Logical 1 during line 17 (in vertical blanking)

Pilot Clock: 2 MHz square wave during VITS 17

KC Key Clamp: logical 1 within horizontal blank

$\overline{ECB}$: logical 0 during composite blanking

Matrix Select: logical 1 = Matrix A2

logical 0 = Matrix A1

Outputs

Red Video, Green Video, Blue Video — 1.5 V pp black positive, restored to ground

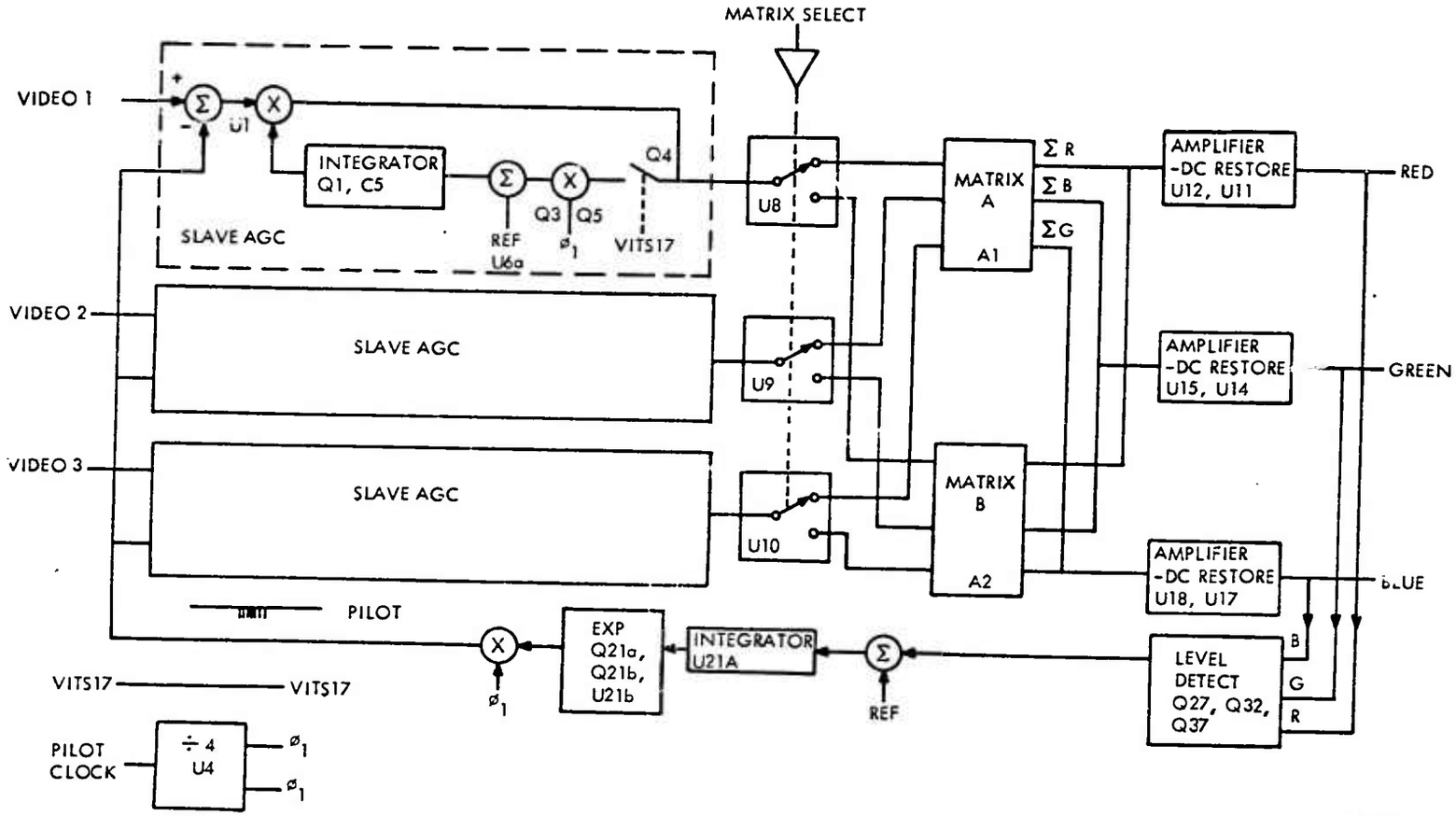
7.5 V Ref, -5V Ref — to gamma corrector on encoder

2.7.2 THEORY OF OPERATION

The block diagram of the color processor is shown in Figure 2-22. The slave AGC adjusts its gain such that the pilot burst is at a reference level at the output of the slave AGC. As the amplitude of the pilot is decreased, the gain will increase proportionally to maintain the output pilot level.

The pilot is a 0.5 MHz square wave occurring on line 17 each field during vertical blanking, with an amplitude between 2 mv and 200 mv. This is summed with Video 1 at the input to U1, which is the gain control stage. As shown in Figure 2-22, during the VITS17 interval, the output current from U1 is gated by Q4 into a synchronous detector consisting of Q3 and Q5, compared to a reference level which is gated on during VITS17 and the difference integrated to give the gain control voltage to U1. If the pilot at the output of U1 is the proper level, the net input to the integrator will be zero, and the control voltage and hence, the gain will be constant. If the gain is either high or low, there will be a net positive or negative input to the integrator, and the gain will change until equilibrium is reached. At times other than VITS17 the integrator input is gated off, and the integrator holds its last output.

In the actual implementation, U1 has a differential current source output. The positive output goes directly to the matrix select switches. The negative output is split into two components, with half directed to the matrix and half used to sense the pilot level. The splitting is done by R2 and R3 into the low impedance common base stage Q6 and the matrix select switch U8. The current is steered into one of three directions by Q3, Q4 and Q5. During the positive portion of the pilot, Q5 is on and the signal pulls C5 negative. During the negative portion of the pilot cycle Q3 is on and the signal current



F2-22

Figure 2-22. Color Processor A7 Block Diagram

2.7.2 (Continued)

is reflected in the current mirror Q1 into C5 with negative gain. Thus C5 will integrate the difference between the positive and negative halves of the cycle, i.e. the peak-peak pilot amplitude. A reference bias current from U6 is on during this interval. When the peak-peak pilot amplitude equals the reference current, there will be no net change in the voltage across C5. Q2 s a gain stage with high impedance input to drive the gain control voltage for U1.

At times when the pilot is off, Q4 is gated on. This directs the output current into a point in the current mirror Q1 such that the Q1 is biased off. This reduces leakage current and allows C5 to hold over the field time of 1/60 second. The peak-peak signal current is 200 ua with 5 ma bias. The gain of the current mirror must be unity to prevent changes in the bias current from appearing as a change in the reference current. This gain is trimmed by R145 Video gain is adjusted by R144.

The green and blue input stages are identical to the red. The positive and negative output currents from the three AGC stages are switched into either of the two plug-in matrices by the transistor arrays U8, U9, and U10. These are essentially common base stages connected for current mode switching.

The matrix must combine the three sensor videos to form Red, Green and Blue video according to:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \begin{bmatrix} V1 \\ V2 \\ V3 \end{bmatrix} \qquad (1)$$

where

R = Red Video
G = Green Video
B = Blue Video
V1 = Video 1
V2 = Video 2
V3 = Video 3

2.7.2 (Continued)

The matrix may have either positive or negative coefficients. The input to the matrix amplifier has only positive gain, requiring that both polarity outputs from the AGC be available.

The matrix amplifiers have a low impedance common base input and the select switches have a high impedance current source output. The matrix consists of a resistor network which splits the current from each of the six AGC outputs into the three matrix amplifiers or ground. The design procedure for the matrix is given in paragraph 2.9.

The Red matrix amplifier consists of a common base stage Q25, a common emitter stage U12D with cascode U12C, a black clipper formed by diode connected U12B and a common emitter state U12A. Current feedback through R44 sets the transimpedance (V_{out}/I_{in}) at 7.5 kilohms. The loop is compensated by by C19.

The output level is 1.5 V pp black positive. Black clip is achieved by the diode clamp U12B. At clip, the current through U12B is approximately the same as the emitter current of U12A, so that the V_{BE} of 12A matches the forward voltage of U12B. The output voltage at clip is thus equal to the voltage across R46. This provides a sharp clip at a well controlled voltage. The black clip is necessary since with a negative matrix coefficient the summed color video may be negative for certain scenes.

2.7.2 (Continued)

A white clip is provided by the limited pulldown current through R50 driving the 1.34 kilohm input resistance of the gamma corrector.

The video output must be DC restored to ground to drive the gamma correctors. During the blanking interval, the output voltage is sampled by Q26 and integrated by U11 and fed back to the input of the matrix amplifier by Q24. The collector of Q24 must carry the summed bias current from the AGC stage, which may be as large as 10 ma before Q24 saturates. R41 sets the level to which video is restored.

Composite blanking is summed with video through R42 to provide a "white" pedestal at the output. This moves the dc restoration voltage away from the black clip level, providing a faster and more linear restoration. The pedestal also provides a noise margin for the blanker in the encoder which can only blank whites.

The remainder of the color processor shown in the block diagram of Figure 2-22. detects the video level and adjusts the pilot magnitude to change gain.

Gain is set such that a preset threshold is exceeded by red, green, or blue video for some fraction of the picture area. This form of peak detection is less sensitive to point overloads.

Any time red, green or blue video exceeds the threshold set by R123 the current from the blanked current source Q42 is switched through Q27, Q32 or Q37 respectively. This current is integrated by U21A. A reference current through R127 is subtracted from the integrator input When steady state is reached, the current from the peak detectors averaged over the field equals the dc reference current. Since the slave AGC's are adjusted once per field,

2.7.2 (Continued)

the integrator output is essentially sampled during vertical blanking. Thus, the influence on gain of a bright area is identical whether the area is at the top or the bottom of the picture.

The exponential function following the integrator is necessary to maintain the loop response time with varying input signal levels. Without it, the response of the loop would be slower for a high input level than for low. The exponential function changes the pilot amplitude and hence slave AGC gain more rapidly for high input for an incremental change in the control voltage from the integrator.

The exponential function is implemented by the base-emitter characteristics of Q21b. Q21a temperature compensates for changes in V_{BE}. The temperature dependence of the transistors collector current with V_{BE} has only a minimal effect on loop gain.

The current from Q21b is chopped to form the pilot by Q19 and Q20. The pilot timing is established by the divide by four counter U4. The pilot clock input is a 2.05 MHz rectangular wave gated on during the pilot interval, VITS line 17 to give a pilot frequency of 0.51 MHz.

2.8 COLOR ENCODER A8 (SK56079-21-12)

The color encoder combines the red, green, and blue video with composite sync and blanking to form composite video compatible with the standards established by the National Television Systems Committee (NTSC). Bandwidths different from NTSC standards have been incorporated to simplify the design while permitting use of a NTSC compatible monitor. (See figure 4-8.)

2.8.1 SUBASSEMBLY INTERFACE

Input:

VIDEO (INTO 1.32K)

Red Video: 1.5VPP, Black Positive, Black = 0V

Green Video: " " " " "

Blue Video: " " " " "

TTL LEVELS (POSITIVE TRUE)

$\overline{BF}$: Burst Flag, Logical 0 during burst

$\overline{CS}$: Composite Sync, Logical 0 during sync

$\overline{CB}$: Composite Blank, Logical 0 during blank

14MHz Clock: 14.31818MHz ±40 Hz squarewave

Output:

Composite Video, 1VPP, Black negative into 75 Ω

Timing and levels compatible with EIA Standard RS-170 and Vol. III of the FCC rules and regulations.

2.8.2 THEORY OF OPERATION

The color properties of the three video signals may be characterized by the terms luminance, hue and saturation. Luminance corresponds to the subjective "brightness" of the light. This is the information displayed as shades of gray in a monochrome system.

2.8.2 (Continued)

The hue of any colored light is commonly referred to by adjectives such as red, yellow, or blue. The physicist defines the hue of a colored light quantitatively as specifying its dominant wavelength. Red hues, for example, have dominant wavelengths in the vicinity of 620 nanometers.

The saturation or, quantitatively, the purity of a colored light, depends upon the white light content, that is, the degree to which white light is not present. For instance, if a quantity of white light were to be mixed with a pure green light, a pastel green of the same hue would result.

The brightness of a light is its apparent intensity. Brightness, however, is a subjective term and should be used only in a nonquantitative sense. Luminance is the proper term for referring to photometric quantities of light.

These properties are generally represented by CIE chromaticity chart and reproduced in figure 2-23 with several examples.

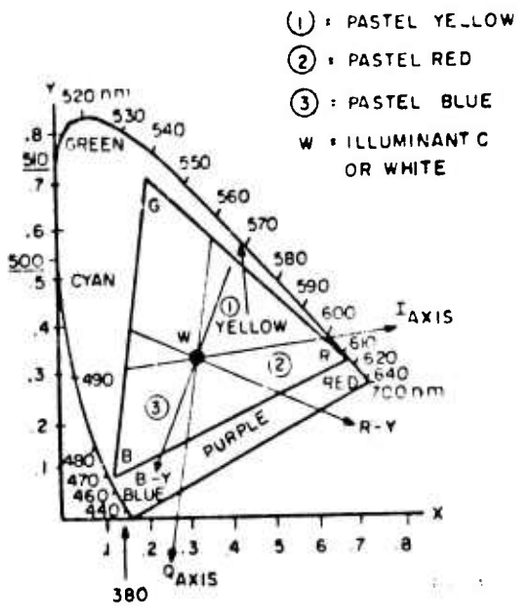


Figure 2-23. Chromaticity Chart

2.8.2 (Continued)

NTSC standards define luminance or Y' as

$$Y' = 0.30R' + 0.59G' + 0.11B' \quad (1)$$

Note that the levels of R', B', and G' are defined such that a reference white (or gray) will produce equal values of R', G', B', and Y'. The primes denote gamma corrected values. The Y' video was assigned to the wide bandwidth main channel under NTSC standards to be displayed by a monochrome monitor as shades of gray.

Chrominance may be thought of as the difference between the luminance and the color to be displayed. Since there are three primary colors there must be two parameters describing chrominance in addition to luminance. The two parameters chosen by NTSC are presented by the linear transformation

$$I' = 0.27\ (B' - Y') + 0.74\ (R' - Y') \quad (2)$$

$$Q' = 0.41\ (B' - Y') + 0.48\ (R' - Y') \quad (3)$$

These chrominance values may be plotted as in figure 2-24, where the dashed axes represent I' and Q'. The hues represented by these axes are indicated in figure 2-23. These axes were chosen to represent the hues for which the eye has the best resolution (I' axis) and the poorest resolution (Q' axis). The I' information then requires more bandwidth than Q' to adequately represent the color picture for interpretation by the human eye. The unequal bandwidths were chosen by NTSC for compatibility with monochrome transmission. There is no need in this application for the bandwidth of the two chrominance channels to be different. If they are the same the mechanization of the encoder is simplified because the delay through the filter will be the same and a trimming delay line may be eliminated.

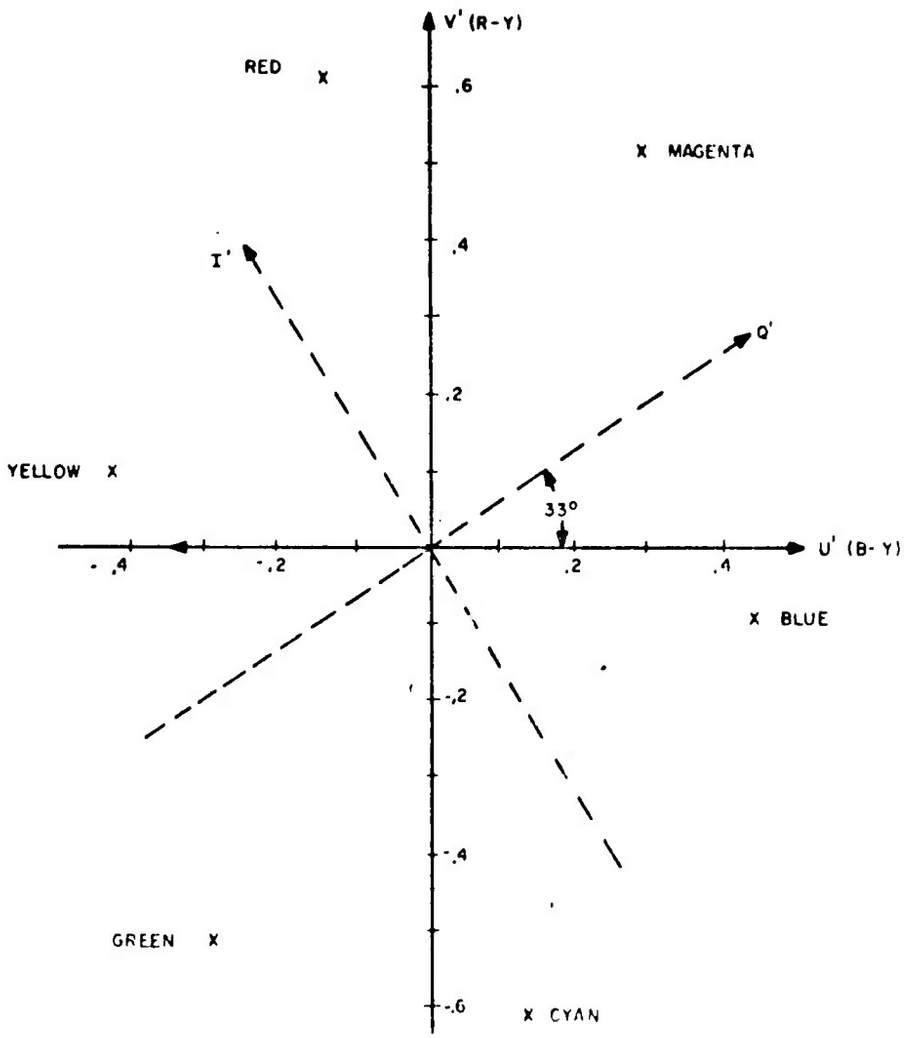


Figure 2-24. Chrominance Phase

2.8.2 (Continued)

For equal chrominance passbands, any set of orthogonal axes in figure 2-24 may be used to encode chrominance with equivalent results, provided that the phase reference is maintained. The proposed design uses the U' - V' axis shown where

$$U' = \frac{1}{2.02}(B' - Y') = \frac{1}{2.02}(.89\ B' - .30R' - .59G') \qquad (4)$$

and

$$V' = \frac{1}{1.14}(R' - Y') = \frac{1}{1.14}(.70R' - .59G' - .11B') \qquad (5)$$

The U' and V' signals are quadrature encoded on a 3.58 MHz subcarrier by double sideband suppressed carrier amplitude modulation. The output of the encoder may thus be represented for low frequencies of U' and V' as

$$Y' + U' \cos \omega_0 t + V' \sin \omega_0 t,$$

where

$$\omega_0 = 2\pi \times 3.58 \text{ MHz}.$$

2.8.3 CIRCUIT DESCRIPTION

Figure 2-25 is the block diagram of the encoder. The three gamma correctors are nonlinear networks which have lower incremental gain for higher signal levels. The purpose of the network is to give a net linear transfer through the system from light input to brightness on the monitor. This is necessary in order to maintain color balance for different shades of gray. The CID is essentially linear over its operating range, thus, the gamma corrector must correct for the monitor nonlinearity. The monitor has a gamma of 2.5, i.e.,

$$\text{Brightness} \propto (V_{input})^{2.5}$$

The gamma corrector must be of the form

$$V_{out} \propto (V_{input})^{0.4}$$

The red gamma corrector will be discussed as typical of the three. U13 is a monolithic transistor array with matched V_{BE}. A simplified schematic is shown in figure 2-26. The three transistors are coupled at the emitter, forming an emitter follower. If the base voltages are different by more than 5-10 mv only one transistor will be conducting. The total emitter follower will thus follow the most positive base voltage. The resistor network R67 to R71 derives the three base voltages as shown in figure 2-27. The video input V1 is 1.5 vpp "white" negative with black at ground. The net input-output transfer follows the shape of the dashed line in figure 2-27.

This form of gamma corrector has the advantage that the nonlinear and temperature dependent characteristics have only a second order effect on the circuit performance, and the three channels will track as closely as the tolerance of the network.

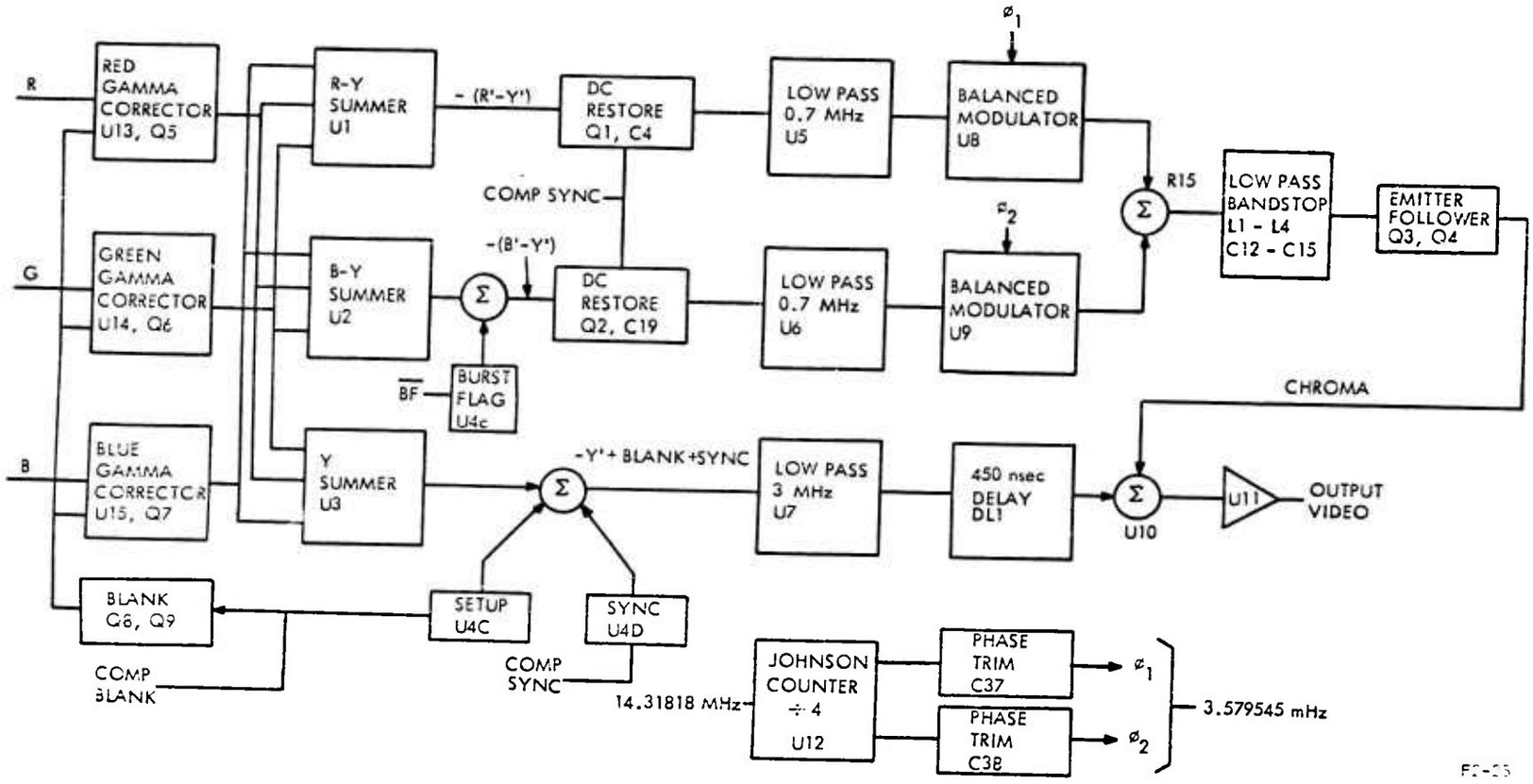


Figure 2-25. Encoder Block Diagram

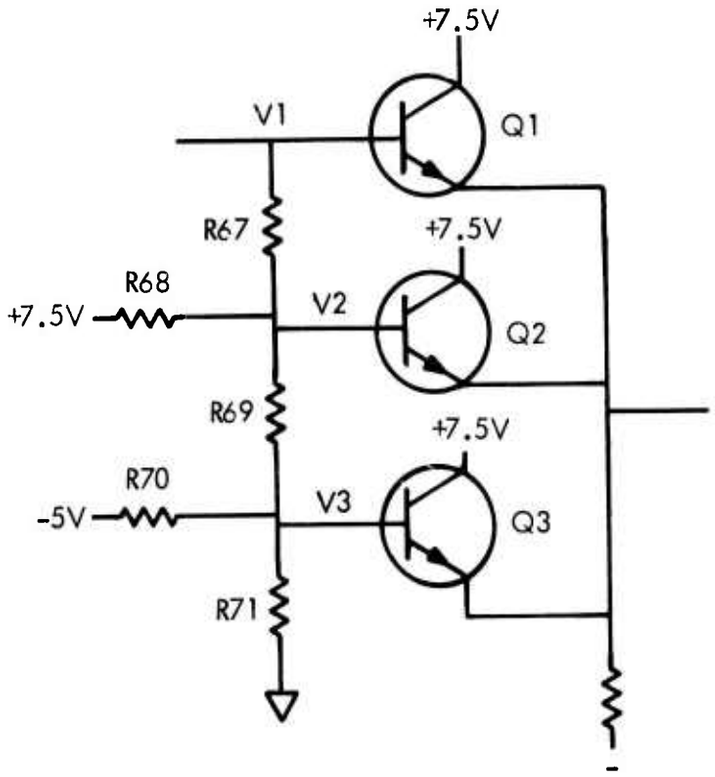


Figure 2-26. Gamma Corrector Simplified Schematic

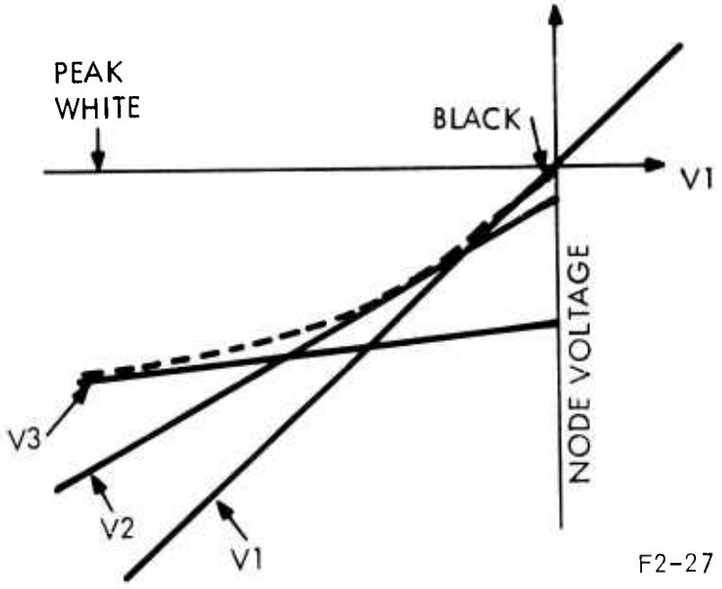


Figure 2-27. Node Voltages as a Function of Input

2.8.3 (Continued)

One of the remaining transistors in U13 (with its base on pin 9) is used to provide a dc offset such that as R74 is adjusted to change gain there is no significant dc shift. Q5 approximately compensates for V_{BE} of U13. The output for 1.5V input is 380 mV (with R74 fully clockwise). Nominal output at TP6 is 200 mv.

The remaining transistor in U13 (base on pin 12) is used for blanking. During blanking, the base is clamped to ground by Q9. During active time, the base is pulled more than 1.5V negative by Q8 and CR1.

The encoder consists of three parallel channels. The U' and V' channels are nearly identical and will be discussed together.

The chrominance difference U' and V' signals are derived in the R-Y and B-Y summers (U1 and U2). These circuits take the weighted sum of the R', B' and G' inputs according to equations (1), (4) and (5). An alternative configuration would derive -Y' according to equation (1) and add this to R' and B' directly. The output is scaled such that peak red, green or blue correspond to -1V, e.g., a 100% red color bar at the input would give -0.7V at the output of U1 and +.3V at the output of U2.

A pulse coincident with the burst envelope is summed with the B-Y channel. This will later be modulated by the subcarrier to form the color burst.

During the blanking interval, the inputs correspond to black. The chroma differences R-Y and B-Y must be restored to 0V within blanking in order to assure that there is no residual subcarrier in blanking. This would shift the burst phase and give a corresponding chromatic change in the display's decoder This is implemented with C4, Q1, C19, and Q2 driven by U4a and U4b.

2.8.3 (Continued)

The R-Y and B-Y signals are passed through 0.7 MHz (3 dB) 2 pole Butterworth active filters consisting of U5, R7, R8, C6, and C7 in the R-Y channel and U6, R26, R27, C21 and C47 for B-Y. This represents a compromise between the rate at which the response falls off (12 dB/octave) and the overshooting on transitions. If a higher order filter is used, it would require a phase corrector to linearize phase shift with frequency, and give symmetric transitions on positive and negative going edges.

The color difference channels are modulated by the 3.58 MHz subcarriers in quadrature by U8 and U9. The input to the modulator must be offset to null the DC offsets from the restorers, low pass filters, and the balanced modulators. The signal gains are not equal, to give the gain required in eqns. 4 and 5.

The subcarriers are derived from a 2 bit Johnson counter (U12) clocked by the same 14.31818 MHz oscillator which clocks the sync generator. The outputs of the Johnson counter are in quadrature to within the difference in propagation delays in the counter. Any difference in the phase may be compensated by selecting a capacitor (C38 or C39) in the attenuator (R51, R53, R55, and R56) which drops the 3V TTL signal to 0.3 Vpp to drive the modulators. Since the burst, which establishes the phase reference is derived by modulating a pulse in the B-Y channel, it will be identically in phase with one of the subcarriers. Thus, the relative phase of the subcarriers is important, but the absolute phase is not. To trim the phase, only one or the other of the subcarriers need be lagged by the phase trim capacitor. There is approximately 22 pF required for each degree of correction.

2.8.3 (Continued)

The two components of the subcarrier are summed to give chrominance in R15, since the outputs of U8 and U9 are current sources. The chroma is passed through a low pass/band stop filter consisting of L1 to L4 and C12 to C15, to remove the harmonics of the subcarriers. Transistor Q3 and Q4 form a temperature compensated emitter follower to provide a low impedance driving point to the luminance-chrominance summer.

The major departure from NTSC standards in the design of the chroma channels lies in the equal passbands chosen for R-Y and B-Y, as opposed to the unequal passbands on I and Q required by NTSC. If the passbands were not equal, the delay thru the filters would not be the same. This would require a delay line and associated drive circuits to equalize the delay. The size and complexity added is not justified, considering the few, if any, monitors have different passbands on the two chroma channels of the decoder.

The third channel in the encoder is for luminance. The gamma corrected videos are summed by U3 according to equation (1) with the output scaled to give 1V with R' = G' = B = Max. Since this channel will have to be delayed to match the chroma delay, sync and blanking will have to be delayed identically. This is done by summing composite blanking and sync in the appropriate proportions to give a composite waveform, minus chroma. The setup is .082V and sync is .432V at the output of U3.

The composite waveform is filtered to 3 MHz by U7 in a filter similar to the chroma filters and delayed by DL1 to equalize the relative delay between the chroma and 150 nsec on luminance, which leaves 450 nsec to be equalized by DL1.

Luminance is summed with chroma in U10, with U11 used as a line driver.

2.9 PLUG-IN MATRIX DESIGN

The matrix must combine the three sensor videos to form Red, Green and Blue video according to:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \begin{bmatrix} V1 \\ V2 \\ V3 \end{bmatrix} \qquad (1)$$

where R = Red Video
G = Green Video
B = Blue Video
V1 = Video 1
V2 = Video 2
V3 = Video 3

Each of the three videos is brought into the matrix with both positive and negative polarity, giving six inputs to the actual matrix. Eqn. 1 may be written

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} & B_{13} & B_{14} & B_{15} & B_{16} \\ B_{21} & B_{22} & B_{23} & B_{24} & B_{25} & B_{26} \\ B_{31} & B_{32} & B_{33} & B_{34} & B_{35} & B_{36} \end{bmatrix} \begin{bmatrix} -V1/2 \\ V1 \\ -V2/2 \\ V2 \\ -V3/2 \\ V3 \end{bmatrix} \qquad (2)$$

where $B_{m,2n} - B_{m,2n-1}/2 = A_{mn}$

and $B_{mn} \geq 0$

As a general rule, either B coefficient or both should be zero.

Each input is a current source which is split into the three video outputs. Depending on the total gain, some of the input current may have to be shunted to ground. If this ground current is treated as a fourth output denoted by 0, Eqn. 2 may be written.

2.9 (Continued)

$$\begin{bmatrix} R \\ G \\ B \\ 0 \end{bmatrix} = \frac{1}{Bo} \begin{bmatrix} B_{11} & B_{12} & B_{13} & B_{14} & B_{15} & B_{16} \\ B_{21} & B_{22} & B_{23} & B_{24} & B_{25} & B_{26} \\ B_{31} & B_{32} & B_{33} & B_{34} & B_{35} & B_{36} \\ B_{41} & B_{42} & B_{43} & B_{44} & B_{45} & B_{46} \end{bmatrix} \begin{bmatrix} -V1/2 \\ V1 \\ -V2/2 \\ V2 \\ -V3/2 \\ V3 \end{bmatrix} \qquad (3)$$

where Bo = normalizing factor > 0

and $B_{4n} = Bo - (B_{1n} + B_{2n} + B_{3n})$

Bo is chosen such that all coefficients are ≥ 0. If at least one B coefficient in the fourth row is equal to zero, maximum matrix gain will result.

Each column of the 4 x 6 matrix in Eqn. 3 represents how the respective current input is split into the three color outputs. The design of the part of the matrix corresponding to a given column of the matrix is essentially independent of the other parts. The configuration for a column is shown in figure 2-28, where a current source is loaded into four resistors. The inputs to the amplifiers are low impedance. The total node impedance is R,

$$R = \frac{1}{1/R_{1n} + 1/R_{2n} + 1/R_{3n} + 1/R_{4n}} \qquad (4)$$

For input current I_n each output current is

$$i_{mn} = I_n R/R_{mn}$$

The desired matrix coefficient for the B matrix of Eqn. 3 is

$$\frac{B_{mn}}{Bo} = \frac{i_{mn}}{I_n} = \frac{R}{R_{mn}}$$

The resistor value is thus

$$R_{mn} = RBo/B_{mn} \qquad (7)$$

The full design procedure is:

1. Establish the nine matrix coefficients in Eqn. 1.
2. Separate each coefficient into two parts depending on the sign of the coefficient as in Eqn. 2.

2.9 (Continued)

3. Sum each column of 3 elements. Take the largest of the six sums as Bo, and set up the 4x6 matrix of Eqn. 3.

4. Calculate the resistor values according to:

$$R_{mn} = \begin{cases} 0 \text{ (wire link) if } B_{mn} = Bo \\ \infty \text{ (open) if } B_{mn} = 0 \\ RBo/B_{mn} \text{ otherwise} \end{cases}$$

choosing R as a convenient value

$$205 \leq R \leq 511$$

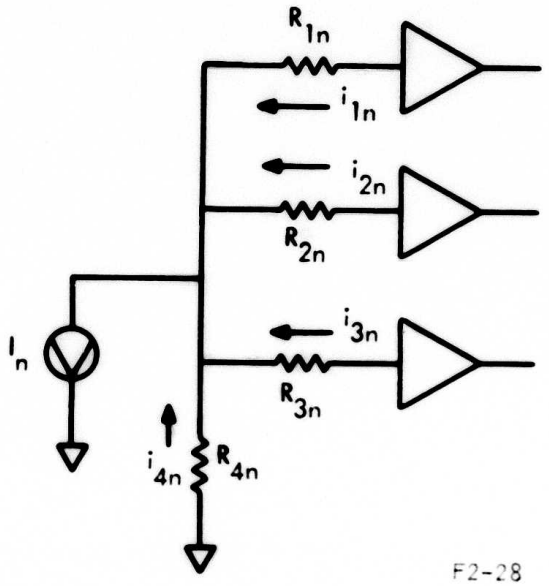


Figure 2-28. Typical Current Input for 4x6 Matrix Column

REPLACEMENT PARTS LISTS

3.1 ORGANIZATION

Parts lists are in subassembly order by reference designator. Electrical parts on subassemblies are listed by reference designator with multiple entries listed by lowest reference designator. Each entry consists of one or more reference designators, part number, and vendor code or remarks as applicable. If the part number is not assigned by military standard, a vendor abbreviation is given under Remarks according to Table 3-1. Parts which are selected in test are denoted by an incomplete part number to indicate the type of part, or a selection criterion is given under Remarks.

The assembly breakdown is given in 2.1.

Table 3-1. Vendor Abbreviation, Address and Code

ABBREVIATION	NAME/ADDRESS	CODE
Airborn	AIRBORN, INC	10400
Allen	ALLEN AVIONICS INC. 224 E 2nd Street Mineola, N.Y. 11501	-
Amp	AMPEREX ELECTRONICS CORP.	73445
Augat	AUGAT, INC.	91506
Automatic	AUTOMATIC METAL PRODUCTS CORP.	94375
Can	ITT CANNON ELECTRIC	71468
Dale	DALE ELECTRONICS INC	91637
Erie	ERIE TECHNOLOGICAL PRODUCTS INC.	72982
FCH	FAIRCHILD SEMICONDUCTOR	07263
GE	GENERAL ELECTRIC	99971
GI	GENERAL INSTRUMENT CORP.	14936
HP	HEWLETT PACKARD CO.	50434
Kraft	KRAFT SYSTEMS INC. 450 West California Avenue Vista, California 92083	-
Mc Coy	MC COY ELECTRONICS CO.	00136
Microdot	MICRODOT INC.	34692
MOT	MOTOROLA INC, SEMICONDUCTOR PROD. DIV.	04713
Nytronics	NYTRONICS COMPONENTS GROUP INC.	00213
NS	NATIONAL SEMICONDUCTOR CORP.	12040
Powercube	POWERCUBE CORPORATION 214 Calvary St. Waltham, Mass 02154	-

Table 3-1. Vendor Abbreviation, Address and Code (Continued)

ABBREVIATION	NAME/ADDRESS	CODE
RCA	RCA CORP.	21921
SIL	SILICONIX	17856
TI	TEXAS INSTRUMENTS INC, Semiconductor Group	02195
WJ	WATKINS-JOHNSON COMPANY	14482

CID Color Camera 1 (SK56079-21-16)

Reference Designator	Part Number	Remarks (Vendor)
A1	SK56079-21-17	
A2	SK56079-21-17	
A3	SK56079-21-17	
A4	SK56079-21-18	
A5	SK56079-21-19	
A6	SK56079-21-20	
A7	SK56079-21-21	
A8	SK56079-21-22	
A9	SK56079-21-23	
J1	SMP20-11	(Dale)
L1	7571516G1	(GE)
C1	M39003/03-0187J	
C2	M39003/03-0187J	
R1	RCR07G181JS	
P1	616-DG5	(Augat)
P2	614-DG5	(Augat)
P3	616-DG5	(Augat)
P4	616-DG5	(Augat)
P5	886C129P6	(GE)
P6	886C129P6	(GE)
P7	886C129P6	(GE)
P8	DCMM-21WA4S-A156	(Can)
P9	616-DG5	(Augat)
PS1	P2D407	(Powercube)
PS2	P2D407	(Powercube)
U1	KPS-12	(Kraft)
U2	KPS-12	(Kraft)

Sensor A1, A2, A3 (SK56079-21-17)

Reference Designator	Part Number	Remarks (Vendor)
C1	M39014/01-0473	
C2	M39014/01-0473	
C3	M39014/01-0473	
C4	M39014/01-0473	
C5	M39014/01-0473	
C6	M39014/01-0473	
C7	CM04FD101JS	
P1	MCDMI-25PS	(Microdot)
R1	RNC50H5110FS	
R2	RNC50H5110FS	
R3	RNC50H1001FS	
R4	RNC50H1001FS	
R5	RNC50H1001FS	
R6	RNC50H1000FS	
R7	RNC50H2150FS	
R8	RNR55	Select
R9	RNR55	Select
U1	SK56079-21-5	Charge Injection Device (CID)

Oscillator A5 (SK56079-21-19)

Reference Designator	Part Number	Remarks (Vendor)
A1	MC380A2-14G 14.31818 MHz	(McCoy)
C1	M39003/01-2259	
P1	WT4SEC	(Airborn)

Drivers A4 (SK56079-21-18)

Reference Designator	Part Number	Remarks (Vendor)
C1	M39003/01-2356	
C2	M39003/01-2268	
C3	M39003/01-2268	
C4	M39003/01-2356	
C5	M39003/01-2304	
C6	M39003/01-2304	
C7	M39014/01-0473	
C8	M39003/01-2242	
C9	M39014/01-0473	
C10	M39014/01-0473	
C11	M39014/01-0473	
C12	M39014/01-0473	
C13	M39014/01-0473	
C14	M39014/01-0473	
C15	M39003/01-2356	
C16	M39003/01-2356	
C17	M39003/01-2356	
C18	M39003/01-2356	
C19	M39003/01-2356	
C20	M39003/01-2356	
C21	M39014/01-0473	
C22	M39014/01-0473	
C23	M39014/01-0473	
C24	M39003/01-2271	
C25	M39003/01-2271	
C26	M39003/01-2271	
C27	M39014/01-2473	
C28	M39014/01-2473	
C34	M39014/01-0473	
C35	M39014/01-0473	
C36	M39014/01-0473	
C37	M39014/01-0473	
C38	M39014/01-0473	
C39	M39014/01-0473	
C41	M39003/01-2283	
C42 to C52	M39014/01-0456	
C53	M39014/01-0473	
CR1	JANTX1N914	
CR2	JANTX1N914	

Drivers A4 (SK56079-21-18) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
CR3	JANTX1N914	
CR4	JANTX1N914	
J1	MCDM1-25S607	(Microdot)
J2	MCDM1-25S607	(Microdot)
J3	MCDM1-25S607	(Microdot)
J4	WT7SER7	(Airborn)
J5	516-AG11D	(Augat)
J6	WT4PC	(Airborn)
Q1	MEM807	(GI)
Q2	MEM711	(GI)
Q3	MEM807	(GI)
Q4	MEM711	(GI)
Q5	MEM807	(GI)
Q6	MEM711	(GI)
Q7	MEM807	(GI)
Q8	MEM711	(GI)
Q9	MEM807	(GI)
Q10	MEM711	(GI)
Q11	MEM807	(GI)
Q12	MEM711	(GI)
Q13	JANTX2N2907A	
R1	RNR55H2371FM	
R2	RNR55H5111FM	
R3	RJ26CW203	
R4	RCR07G220JS	
R5	RNR55H2371FM	
R6	RNR55H5111FM	
R7	RJ26CW203	
R8	RCR07G4R7JS	
R9	RNR55H2150FM	
R10	RJ26CW502	
R11	RNR55H2152FM	
R12	RNR55H1001FM	
R13	RNR55H1622FM	
R14	RNR55H1001FM	
R15	RJ26CW501	
R16	RJ26CW501	
R17	RJ26CW501	

Drivers A4 (SK56079-21-18) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
R18	RJ26CW501	
R19	RJ26CW501	
R20	RJ26CW501	
R21	RNR55H3322FM	
R22	RNR55H3322FM	
R23	RNR55H3322FM	
R24	RNR55H3322FM	
R25	RNR55H3322FM	
R26	RNR55H3322FM	
R27	RCR07G103JS	
R28	RCR07G103JS	
R29	RWR81S1210FM	
R45	RNR55H3831FM	
R46	RNR55H3831FM	
R47	RJ26CW201	
R48	RNR55H3831FM	
R49	RNR55H3831FM	
R50	RJ26CW201	
R51	RNR55H3831FM	
R52	RNR55H3831FM	
R53	RJ26CW201	
R54	RCR07G472JS	
R55	RJ26CW102	
R56	RJ26CW102	
R57	RJ26CW102	
R58	RCR07G472JS	
R59	RNR55H1000FM	
R60	RNR55H1000FM	
R61	RNR55H1000FM	
R62	RNR55H1000FM	
R63	RNR55H1000FM	
R64	RNR55H1000FM	
R65	RNR55H51R1FM	
R66	RNR55H51R1FM	
R67	RNR55H51R1FM	
U1	SN54163J	(TI)
U2	SN54LS113	(TI)
U3	MM5320N	(NS)
U4	SN5493AJ	(TI)

Drivers A4 (SK56079-21-18) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
U5	SN54LS175J	(TI)
U6	SN54LS175J	(TI)
U7	SN54S175J	(TI)
U8	SN54S175J	(TI)
U9	SN54LS113J	(TI)
U10	SN54LS21J	(TI)
U11	SN5428J	(TI)
U12	SN5437J	(TI)
U13	SN54LS04J	(TI)
U14	SN54LS08J	(TI)
U15	SN54LS00J	(TI)
U16	SN54LS08J	(TI)
U17	SN54LS04J	(TI)
U18	SN54LS04J	(TI)
U19	SN54LS08J	(TI)
U20	SN54LS08J	(TI)
U21	SN54LS00J	(TI)
U22	SN54LS113J	(TI)
U23	LM104H	(NS)
U24	LM104H	(NS)
U25	741HM	(FCH)
U26	ATF472	(AMP)
U27	ATF472	(AMP)
U28	MH0007H	(NS)
U29	MH0007H	(NS)
U30	DH0034H	(NS)
U31	DH0034M	(NS)
U32	DH0034M	(NS)
U33	ATF472	(AMP)
U34	ATF473	(AMP)
U35	ATF472	(AMP)
VR1	JANIN746	

Preamplifier A6 (SK56079-21-20)

Reference Designator	Part Number	Remarks (Vendor)
C1,C24,C47	M39014/01-0455	
C2,C25,C48	M39014/01-0455	
C3,C26,C49	M39014/01-0455	
C4,C27,C50	M39014/01-0455	
C5,C28,C51	M39014/01-0455	
C6,C29,C52	M39014/01-0455	
C7,C30,C53	M39014/01-0455	
C8,C31,C54	M39014/01-0455	
C9,C32,C55	M39014/01-0455	
C10,C33,C56	M39014/01-0455	
C11,C34,C57	CM04ED470J03	
C12,C35,C58	CM04ED470J03	
C13,C36,C59	M39014/01-0477	
C14,C37,C60	M39014/01-0477	
C15,C38,C61	CM04ED470J03	
C16,C39,C62	CM04ED470J03	
C17,C40,C63	M39014/01-0474	
C18,C41,C64	M39014/01-0474	
C19,C42,C65	M39014/01-0474	
C20,C43,C66	M39014/01-0474	
C21,C44,C67	CM04ED470J03	
C22,C45,C68	M39014/01-0474	
C23,C46,C69	M39014/01-0474	
C70	M39014/01-6474	
C71	M39014/01-6474	
C72	M39003/01-2356	
C73	M39003/01-2254	
C74	M39003/01-2254	
C75,C76,C77	M39003/01-2242	
CR1	5082-2813	(HP)
CR2	5082-2813	(HP)
CR3	5082-2813	(HP)
CR4	5082-2813	(HP)
CR5	5082-2813	(HP)
CR6	5082-2813	(HP)
J1	514-AG11D	(Augat)
J2	WT7P7	(Airborn)

Preamplifier A6 (SK56079-21-20) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
Q1,Q7,Q13	JANTX2N4959	
Q2,Q8,Q14	JANTX2N4959	
Q3,Q9,Q15	JANTX2N2920	
Q4,Q10,Q16	JANTX2N3810A	
Q5,Q11,Q17	JANTX2N5545	
Q6,Q12,Q18	JANTX2N2920	
R1,R31,R61	RCR07G151JS	
R2,R32,R62	RCR07G151JS	
R3,R33,R63	RNR55H4021FM	
R4,R34,R64	RNR55H4021FM	
R5,R35,R65	RNR55H4021FM	
R6,R36,R66	RNR55H4021FM	
R7,R37,R67	RNR55H4021FM	
R8,R38,R68	RNR55H4021FM	
R9,R39,R69	RNR55H2051FM	
R10,R40,R70	RNR55H2051FM	
R11,R41,R71	RJ26CW502	
R12,R42,R72	RJ26CW502	
R13,R43,R73	RNR55H1002FM	
R14,R44,R74	RNR55H1002FM	
R15,R45,R75	RNR55H1781FM	
R16,R46,R76	RNR55H1781FM	
R17,R47,R77	RNR55H1272FM	
R18,R48,R78	RNR55H1272FM	
R19,R49,R79	RNR55H5111FM	
R20,R50,R80	RNR55H5111FM	
R21,R51,R81	RNR55H7500FM	
R22,R52,R82	RNR55H7500FM	
R23,R53,R83	RNR55H7500FM	
R24,R54,R84	RNR55H7500FM	
R25,R55,R85	RNR55	Select
R26,R56,R86	RNR55	Select
R27,R57,R87	RNR55H9092FM	
R28,R58,R88	RNR55H9092FM	
R29,R59,R89	RJ26CW103	
R30,R60,R90	RJ26CW103	
R92,R94,R96	RNR55H2213FM	
R93,R95,R97	RNR55H2213FM	
R98,R99,R100	RNR55H5111FM	

Preamplifier A6 (SK56079-21-20) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
T1	BT8C	(WJ)
T2	BT8C	(WJ)
T3	BT8C	(WJ)
U1,U4,U7	733HM	(FCH)
U2,U5,U8	733HM	(FCH)
U3,U6,U9	LH0002	(NS)
U10	CD4016AN	(RCA)
U11	CD4016AN	(RCA)
U12	CD4016AN	(RCA)
U13	CD4016AN	(RCA)
U14	SN5437J	(TI)
U15	ATF472	(Amp)
VR1	1N751A	

Color Processor A7 (SK56079-21-21)

Reference Designator	Part Number	Remarks (Vendor)
A1	SK56079-21-24	Selected plug-in matrix
A2	SK56079-21-24	Selected plug-in matrix
C1, C6, C11	M39003/01-2289	
C2, C7, C12	M39003/01-2289	
C3, C8, C13	M39014/01-0473	
C4, C9, C14	M39014/01-0473	
C5, C10, C15	M39014/01-0473	
C16	M39014/01-0473	
C17, C22, C27	M39014/01-0473	
C18, C23, C28	M39003101-2304	
C19, C24, C29	CM04ED101 J03	
C20, C25, C30	M39014/01-0473	
C21, C26, C31	M39014/01-0473	
C32	M39014/02-0407	
C33	M39014/02-0407	
C34	M39014/01-0473	
C35	M39014/01-0473	
C36	M39003/01-2304	
C37	M39003/01-2304	
C38	M39003/01-2254	
C39	M39003/01-2289	
C40	M39014/01-0473	
C41	M39003/01-2289	
C42	M39014/01-0473	
C43	M39014/01-0473	
CR1	JANTX1N5711	
CR2, CR3, CR4	JANTX1N914	
CR5	JANTX1N5711	
CR6	JANTX1N5711	
CR7	JANTX1N914	
J1	516-AG11D	(Augat)
J2	516-AG11D	(Augat)
J3	516-AG11D	(Augat)
J4	516-AG11D	(Augat)
J5	886C129P1	(GE)
J6	886C129P1	(GE)
J7	886C129P1	(GE)

Color Processor A7 (SK56079-21-21) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
Q1, Q7, Q13	JANTX2N3810A	
Q2, A8, Q14	JANTX2N2609	
Q3, Q9, Q15	JANTX2N2222A	
Q4, Q10, Q16	JANTX2N2222A	
Q5, Q11, Q17	JANTX2N2222A	
Q6, Q12, Q18	JANTX2N2222A	
Q19	JANTX2N2222A	
Q20	JANTX2N2222A	
Q21	JANTX2N2920	
Q22	CR150	(SIL)
Q23	JANTX2N2907A	
Q24, Q29, Q34	JANTX2N2907A	
Q25, Q30, Q35	JANTX2N2907A	
Q26, Q31, Q36	JANTX2N2609	
Q27, Q32, Q37	JANTX2N2907A	
Q41,	JANTX2N2219A	
Q42	JANTX2N2907A	
Q43	JANTX2N2907A	
Q44	JANTX2N2907A	
Q46	JANTX2N2905A	
Q47	JANTX2N2907A	
R1, R9, R17	RNR55H8252FM	
R2, R10, R18	RNR55H5110FM	
R3, R11, R19	RNR55H5110FM	
R4, R12, R20	RCR07G513JS	
R5, R13, R21	RNR55H1001FM	
R6, R14, R22	RNR55H1001FM	
R7, R15, R23	RCR07G511JS	
R8, R16, R24	RCR07G103JS	
R25,	RNR55H1002FM	
R26	RNR55H2052FM	
R27	RCR07G512JS	
R28	RNR55H3321FM	
R29	RNR55H1272FM	
R30	RCR07G133JS	
R31	RCR07G202JS	
R32	RNR55H2150FM	
R33	RNR55H8252FM	
R34	RNR55H1211FM	

Color Processor A7 (SK56079-21-21)(Continued)

Reference Designator	Part Number	Remarks (Vendor)
R35	RCR07G471JS	
R36	RCR07G103JS	
R37, R61, R85	RCR07G681JS	
R38, R62, R86	RCR07G512JS	
R39, R63, R87	RNR55H9092FM	
R40, R64, R88	RNR55H5901FM	
R41, R65, R89	RJ26CW103	
R42, R66, R90	RNR55H1783FM	
R43, R67, R91	RCR07G101JS	
R44, R68, R92	RNR55H7501FM	
R45, R69, R93	RNR55H9091FM	
R46, R70, R94	RNR55H51R1FM	
R47, R71, R95	RNR55H2491FM	
R48, R72, R96	RNR55H90R9FM	
R49, R73, R97	RCR07G512JS	
R50, R74, R98	RNR55H9091FM	
R51, R75, R99	RNR55H5111FM	
R52, R76, R100	RNR55H	Select
R53, R77, R101	RCR07G101JS	
R54, R78, R102	RCR07G101JS	
R55, R79, R103	RCR07G101JS	
R56, R80, R104	RCR07G101JS	
R57, R81, R105	RCR07G101JS	
R109	RCR07G102JS	
R111	RCR07G202JS	
R116	RCR07G512JS	
R117	RCR07G102JS	
R118	RJ26CW202	
R119	RNR55H2741FM	
R120	RNR55H1002FM	
R121	RNR55H1622FM	
R122	RNR55H1101FM	
R123	RJ26CW501	
R124	RNR55H4020FM	
R125	RJ26CW104	
R126	RNR55H5111FM	
R127	RNR55H1003FM	
R128	RJ26CW203	
R129	RCR07G512JS	
R130	RCR07G103JS	

Color Processor A7 (SK56079-21-21)(Continued)

Reference Designator	Part Number	Remarks (Vendor)
R131	RNR55H1962FM	
R132	RNR55H1003FM	
R133	RNR55H8252FM	
R134	RCR07G512JS	
R135	RCR07G102JS	
R136	RCR07G102JS	
R137	RCR07G102JS	
R138	RCR07G102JS	
R139	RCR07G103JS	
R140	RCR07G472JS	
R141	RNR55H2051FM	
R142	RNR55H3011FM	
R143, R146, R149	RNR55H75ROFM	
R144, R147, R150	RJ26CW104	
R145, R148, R151	RJ26CW101	
R152	RNR55H1622FM	
R153, R155, R157	RCR07G471JS	
R159	RCR07G102JS	
R160	RCR07G202JS	
R161	RCR07G202JS	
R164, R165, R166	RCR07G103JS	
R167	RCR07G102JS	
R168	RCR07G133JS	
R169	RCR07G4R7JS	
R170	RCR07G4R7JS	
R171	RCR07G201JS	
R172, R173, R174	RNR55H75ROFM	
R175	RCR07G102JS	
R176	RCR07G102JS	
R177 to R187	RCR07G102JS	
U1, U2, U3	MC1590G	(MOT)
U4	SN54LS113J	(TI)
U5	SN5416J	(TI)
U6	CA3045	(RCA)
U8	LM3045D	(NS)
U9	LM3045D	(NS)
U10	LM3045D	(NS)
U11, U14, U17	741HM	(FCH)

Color Processor A7 (SK56079-21-21)(Continued)

Reference Designator	Part Number	Remarks (Vendor)
U12, U15, U18	CA3146	(RCA)
U20	747HM	(FCH)
U21	747HM	(FCH)
VR1	JANTX1N821	

Encoder A8 (SK56079-21-22)

Reference Designator	Part Number	Remarks (Vendor)
C1	CM04CD100D03	
C2	M39014/01-0474	
C3	M39014/01-0474	
C4	M39014/01-0474	
C5	M39014/01-0455	
C6	CM04FA301F03	
C7	CM04FD151F03	
C8	M39014/01-0474	
C9	M39014/01-0474	
C10	M39003/01-2268	
C11	M39003/01-2304	
C12	CM04FD221J03	
C13	CM04ED220J03	
C14	CM04ED680J03	
C15	CM04ED220J03	
C16	M39014/01-0474	
C17	CM04CD100D03	
C18	M39014/01-0474	
C19	M39014/01-0474	
C20	CM04FA330J03	
C21	CM04FD151F03	
C22	M39014/01-0474	
C23	M39014/01-0474	
C24	CM04CD100D03	
C25	M39014/01-0474	
C26	M39014/01-0474	
C27	CM04CD100D03	
C28	M39014/01-0474	
C29	M39014/01-0474	
C30	CM04FA301J03	
C31	CM04ED750F03	
C32	CM04FD151F03	
C33	M39014/01-0474	
C34	M39014/01-0474	
C35	M39014/02-0220	
C36	M39014/01-0474	
C37	CM04	Select
C38	M39014/02-0220	
C39	CM04	Select
C40	M39003/04-2304	

Encoder A8 (SK56079-21-22) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
C41	M39003/01-2304	
C42	M39003/01-2254	
C43	M39014/02-0220	
C44	M39014/02-0220	
C45	M39014/01-0474	
C46	M39014/01-0474	
C47	CM04FA301F03	
C48	M39014/01-0474	
C49	M39014/01-0474	
C50	M39014/01-0474	
C51	M39014/01-0474	
C52	M39014/01-0474	
C53	M39014/01-0474	
DL1	TD450Z1000	(Allen)
CR1	IN5711	(HP)
J1	DCM-21WA4P-A156-F115	(Can)
J2	RF5585AA8	(Automatic)
L1	MS18130-24	
L2	MS75052-2	
L3	MS75052-2	
L4	MS18130-24	
Q1	JANTX2N2609	
Q2	JANTX2N2609	
Q3	JANTX2N2907A	
Q4	JANTX2N2222A	
Q5	JANTX2N2907A	
Q6	JANTX2N2907A	
Q7	JANTX2N2907A	
Q8	JANTX2N2907A	
Q9	JANTX2N4860	
R1	RNR55H9091FM	
R2	RNR55H1691FM	
R3	RNR55H1431FM	
R4	RNR55H4871FM	

Encoder A8 (SK56079-21-22) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
R5	RNR55H4871FM	
R6	RNR55H1001FM	
R7	RNR55H1001FM	
R8	RNR55H1001FM	
R9	RJ26CW203	
R10	RNR55H1001FM	
R11	RCR07G361JS	
R12	RJ26CW102	
R13	RNR55H6811FM	
R14	RNR55H1001FM	
R15	RNR55H1001FM	
R16	RNR55H1001FM	
R17	RNR55H1001FM	
R18	RNR55H3321FM	
R19	RNR55H1691FM	
R20	RNR55H1101FM	
R21	RNR55H5621FM	
R22	RNR55H4871FM	
R23	RNR55H4021FM	
R24	RNR55H1623FM	
R25	RNR55H4021FM	
R26	RNR55H1001FM	
R27	RNR55H1001FM	
R28	RJ26CW203	
R29	RNR55H1001FM	
R30	RJ26CW102	
R31	RNR55H1781FM	
R32	RNR55H6811FM	
R33	RNR55H7501FM	
R34	RNR55H7501FM	
R35	RNR55H3651FM	
R36	RNR55H1002FM	
R37	RNR55H68R1FM	
R38	RNR55H6810FM	
R39	RNR55H3830FM	
R40	RNR55H1873FM	
R41	RNR55H1781FM	
R42	RNR55H1780FM	
R43	RNR55H3322FM	
R44	RNR55H1051FM	

Encoder A8 (SK56079-21-22) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
R45	RNR55H4021FM	
R46	RNR55H5110FM	
R47	RNR55H5110FM	
R48	RNR55H1001FM	
R49	RNR55H1001FM	
R50	RJ26CW102	
R51	RNR55H1001FM	
R52	RNR55H1471FM	
R53	RNR55H1000FM	
R54	RNR55H1001FM	
R55	RNR55H1001FM	
R56	RNR55H1000FM	
R57	RNR55H4021FM	
R58	RNR55H3162FM	
R59	RNR55H1000FM	
R60	RNR55H3162FM	
R61	RNR55H1000FM	
R62	RNR55H1001FM	
R63	RNR55H1621FM	
R64	RCR07G302JS	
R65	RCR07G302JS	
R66	RCR07G302JS	
R67	RNR55H1001FM	
R68	RNR55H2052FM	
R69	RNR55H1740FM	
R70	RNR55H2551FM	
R71	RNR55H1540FM	
R72	RNR55H1332FM	
R73	RNR55H1332FM	
R74	RJ26CW102	
R75	RCR07G752JS	
R76	RNR55H1001FM	
R77	RNR55H2052FM	
R78	RNR55H1740FM	
R79	RNR55H2551FM	
R80	RNR55H1540FM	
R81	RNR55H1332FM	
R82	RNR55H1332FM	
R83	RJ26CW102	
R84	RCR07G752JS	

Encoder A8 (SK56079-21-22) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
R85	RNR55H1001FM	
R86	RNR55H2052FM	
R87	RNR55H1740FM	
R88	RNR55H2551FM	
R89	RNR55H1540FM	
R90	RNR55H1332FM	
R91	RNR55H1332FM	
R92	RJ26CW102	
R93	RCR07G752JS	
R94	RCR07G101JS	
R95	RCR07G101JS	
R96	RCR07G101JS	
R97	RCR07G10R0JS	
R98	RCR07G10R0JS	
R99	RCR07G202JS	
R100	RNR55H1001FM	
R101	RNR55H2490FM	
R102	RCR07G102JS	
R103	RCR07G102JS	
R104	RCR07G102JS	
U1	CA3100T	(RCA)
U2	CA3100T	(RCA)
U3	CA3100T	(RCA)
U4	SN5416J	(TI)
U5	LM210H	(NS)
U6	LM210H	(NS)
U7	LM210H	(NS)
U8	MC1596G	(MOT)
U9	MC1596G	(MOT)
U10	CA3100T	(RCA)
U11	LH0002H	(NS)
U12	SN54S113J	(TI)
U13	LM3045D	(NS)
U14	LM3045D	(NS)
U15	LM3045D	(NS)
VR1	JANTXIN756	

FPN Canceler A9 (SK56079-21-03)

Reference Designator	Part Number	Remarks (Vendor)
C1,C30,C59	M39014/01-0455	
C2,C31,C60	M39014/01-0474	
C3,C32,C61	M39014/01-0474	
C4,C33,C62	CM04ED470J03	
C5,C34,C63		8-50pF variable, ceramic
C6,C35,C64	M39014/01-0455	
C7,C36,C65	M39014/01-0474	
C8,C37,C66	M39014/01-0474	
C9,C38,C67	M39014/01-0474	
C10,C39,C68	CM04ED470J03	
C11,C40,C69	CM04ED220J03	
C12,C41,C70	M39014/01-0474	
C13,C42,C71	M39003/01-2261	
C14,C43,C72	M39003/01-2254	
C15,C44,C73	M39003/01-2254	
C16,C45,C74	CM04ED200J03	
C17,C46,C75	M39014/01-0474	
C18,C47,C76	M39014/01-0474	
C19,C48,C77	CM04CD120J03	
C20,C49,C78	M39003/01-2283	
C21,C50,C79	CM04CD010D03	
C22,C51,C80	CM04ED470J03	
C24,C53,C82	M39003/01-2249	
C25,C54,C83	15-60F	(Erie)
C26,C55,C84	M39003/01-2254	
C27,C56,C85	CM06FD511J03	
C28,C57,C86	CM06FD102J03	
C29,C58,C87	CM06FD511J03	
CR1,CR3,CR5	JANTX1N914	
CR2,CR5,CR6	JANTX1N914	
DL1,DL3,DL5	DL57	(Amp)
DL2,DL4,DL6	WL20-Z500	(Nytronics)
J1	516-AG11D	(Augat)
L1,L9,L17	MS75052-1	
L2,L10,L18	MS75052-1	
L3,L11,L19	MS18130-24	
L4,L12,L20	MS90537-17	

FPN Canceler A9 (SK56079-21-23) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
L5, L13, L21	MS18130-17	
L6, L14, L22	MS18130-17	
L7, L15, L23	MS18130-20	
L8, L16, L24	MS18130-20	
Q1, Q8, Q15	JANTX2N2222A	
Q2, Q9, Q16	JANTX2N2222A	
Q3, Q10, Q17	JANTX2N2222A	
Q4, Q11, Q18	JANTX2N2907A	
Q5, Q12, Q19	JANTX2N2222A	
Q6, Q13, Q20	2N4860	Select for Vp < 3v
Q7, Q14, Q21	JANTX2N2222A	
R1, R58, R115	RCR07G221JS	
R2, R59, R116	RCR07G681JS	
R3, R60, R117	RCR07G101JS	
R4, R61, R118	RCR07G820JS	
R5, R62, R119	RN55	Select
R6, R63, R120	RCR07G101JS	
R7, R64, R121	RCR07G122JS	
R8, R65, R122	RN55H6811FS	
R9, R66, R123	RNC55H4020FS	
R10, R67, R124	RNC55H1471FS	
R11, R68, R125	RCR07GF222JS	
R12, R69, R126	RNC55H1001FS	
R13, R70, R127	RNC55H4021FS	
R14, R71, R128	RCR07G471JS	
R15, R72, R129	RCR07G471JS	
R16, R73, R130	RCR07G330JS	
R17, R74, R131	RCR07G331JS	
R18, R75, R132	RCR07G221JS	
R19, R76, R133	RCR07G102JS	
R20, R77, R134	RNC55H6810FS	
R21, R78, R135	RNC55H5110FS	
R22, R79, R136	RCR07G101JS	
R23, R80, R137	RNC55H2051FS	
R24, R81, R138	RNC55H6811FS	
R25, R82, R139	RCR07G202JS	
R26, R83, R140	RCR07G101JS	
R27, R84, R141	RCR07G222JS	
R28, R85, R142	RJ26CW502	

FPN Canceler A9 (SK56079-21-23) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
R29,R86,R143	RNC55H1001FS	
R30,R87,R144	RNC55H3010FS	
R31,R88,R145	RNC55H1003FS	
R32,R89,R146	RJ26CW203	
R33,R90,R147	RNC55H5110FS	
R34,R91,R148	RCR07G471JS	
R35,R92,R149	RCR07G471JS	
R36,R93,R150	RCR07G470JS	
R37,R94,R151	RCR07G223JS	
R38,R95,R152	RCR07G5111FS	
R39,R96,R153	RJ26CW203	
R40,R97,R154	RNC55H1003FS	
R41,R98,R155	RJ26CW203	
R42,R99,R156	RNC55H2152FS	
R43,R100,R157	RCR07G472JS	
R44,R101,R158	RNC55H1272FS	
R45,R102,R159	RNC55H2051FS	
R46,R103,R160	RCR07G472JS	
R47,R104,R161	RCR07G102JS	
R48,R105,R162	RCR07G101JS	
R49,R106,R163	RCR07G332JS	
R50,R107,R164	RCR07G242JS	
R51,R108,R165	RNC55H68R1FS	
R52,R109,R166	RCR07G332JS	
R53,R110,R167	RNC55H5110FS	
R54,R111,R168	RCR07G101JS	
R55,R112,R169	RNC55H2051FS	
R56,R113,R170	RNC55H2051FS	
R57,R114,R171	RCR07G104JS	
R172,R176,R180	RCR07G102JS	
R173,R177,R181	RJ26CW502	
R174,R178,R182	RNC55H1001FS	
R175,R179,R183	RNC55H3010FS	
U1,U6,U11	MC1596G	(MOT)
U2,U7,U12	LH0002	(NS)
U3,U8,U13	MC1596G	(MOT)
U4,U9,U14	MC1545G	(MOT)
U5,U10,U15	CA3100T	(RCA)
U16	SN54LS113J	(TI)
U17	SN54LS04J	(TI)

FPN Canceler A9 (SK56079-21-23) (Continued)

Reference Designator	Part Number	Remarks (Vendor)
VR1, VR5, VR9	JANTXIN755A	
VR2, VR6, VR10	JANTXIN755A	
VR3, VR7, VR11	JANTX1N755A	
VR4, VR8, VR12	JANTX1N755A	

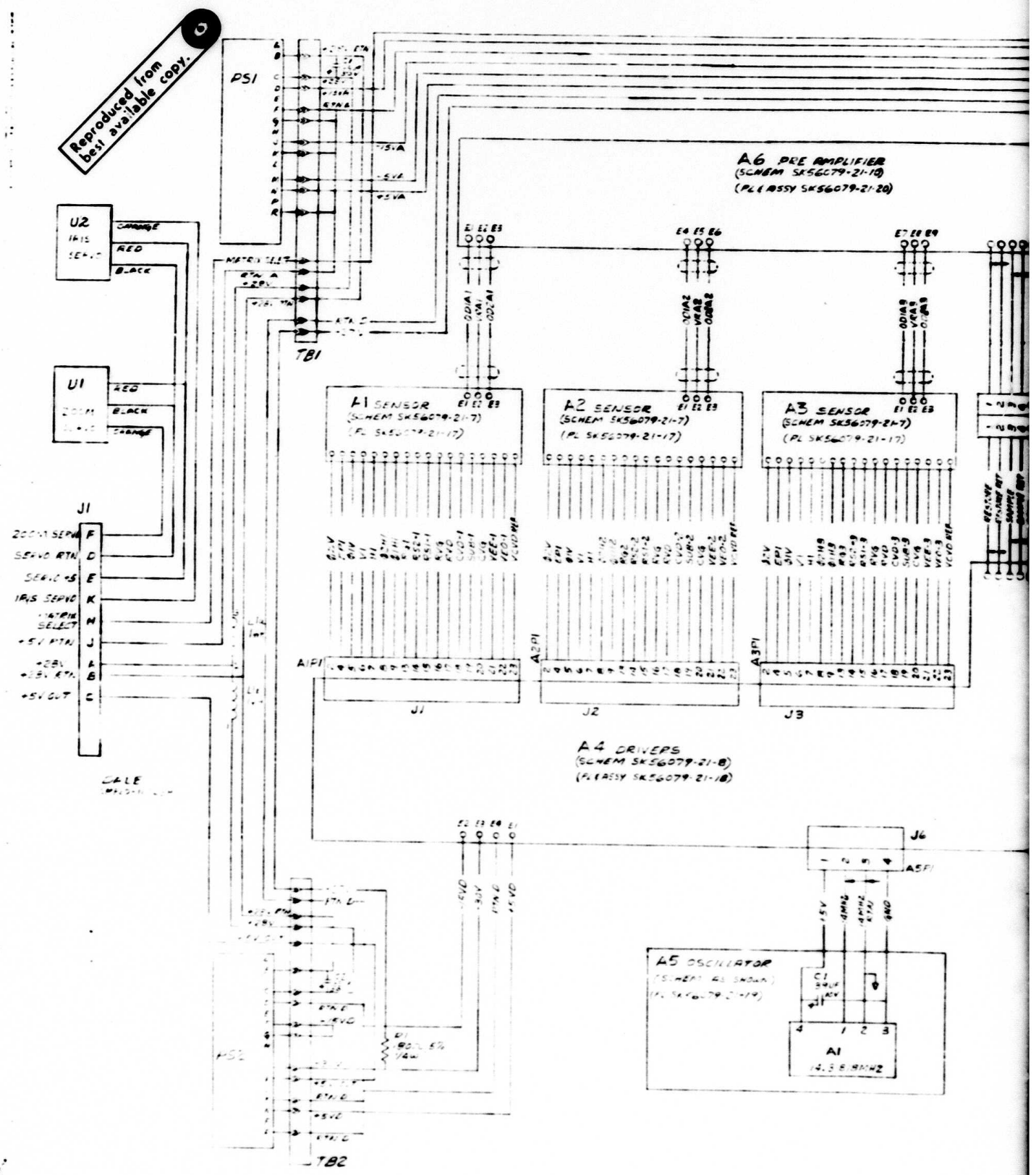
SECTION IV

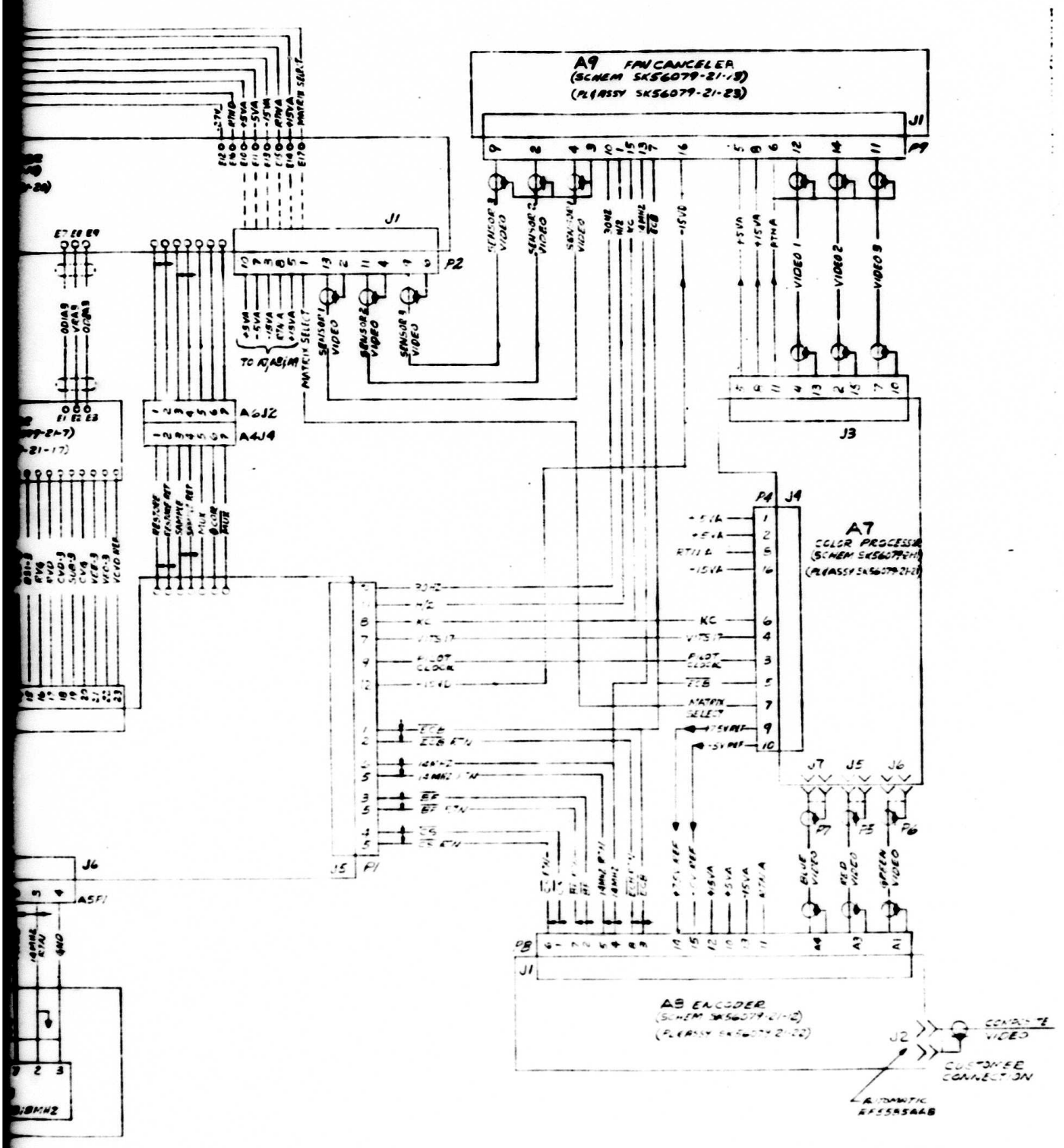
SCHEMATICS

4.1 ORGANIZATION

The schematic diagrams for the CID Color Camera are organized in sub-assembly order with two exceptions. The Oscillator A4 is part of the camera interconnection diagram Figure 4-1, and the Canceler A9 is located between A6 and A7.

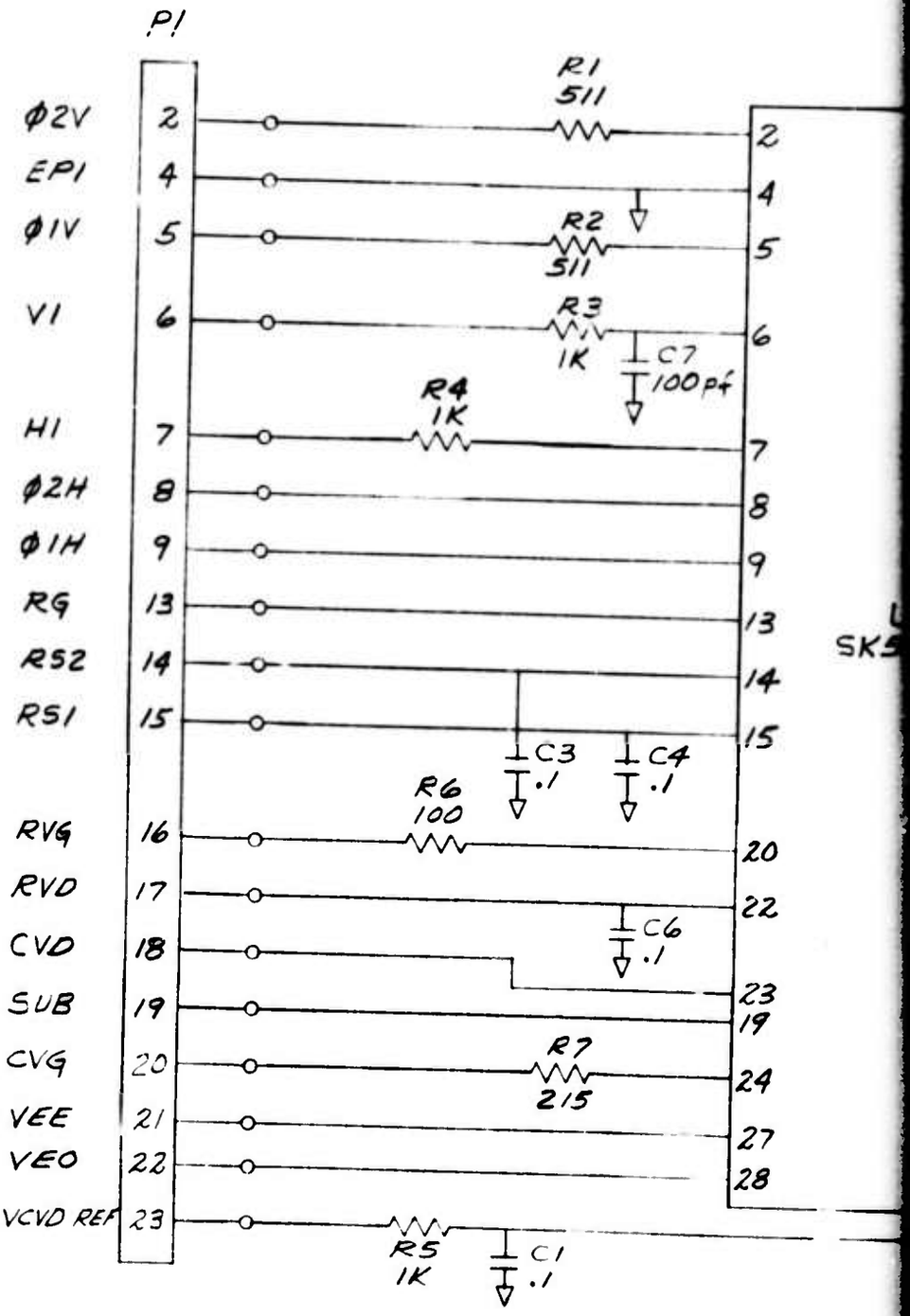
An index to the schematic diagrams which cross-reference the theory of operation and the assembly drawings is given in Table 2-1.





B

Figure 4-1. Interconnection Diagram (SK56079-21-6)


P1
ΦZV
EP1
ΦIV
VI
HI
ΦZH
ΦIH
RG
RS2
RS1
RVG
RVD
CVD
SUB
CVG
VEE
VEO
VCVD REF
2
4
5
6
7
8
9
13
14
15
16
17
18
19
20
21
22
23
R1 511
R2 511
R3 1K
C7 100pf
R4 1K
C3 .1
C4 .1
R6 100
C6 .1
R7 215
R5 1K
C1 .1
2
4
5
6
7
8
9
13
14
15
20
22
23
19
24
27
28
SK5

A

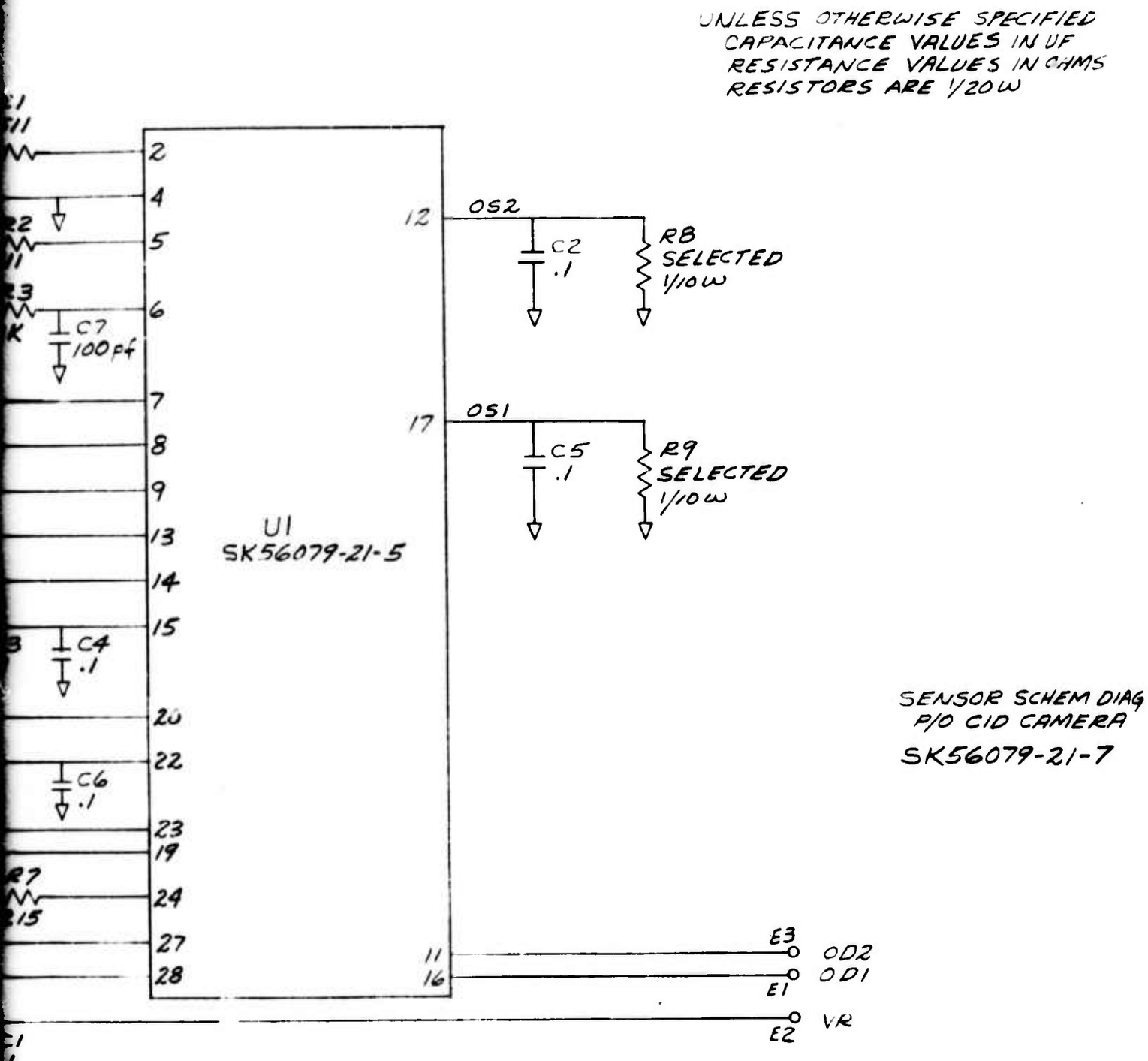
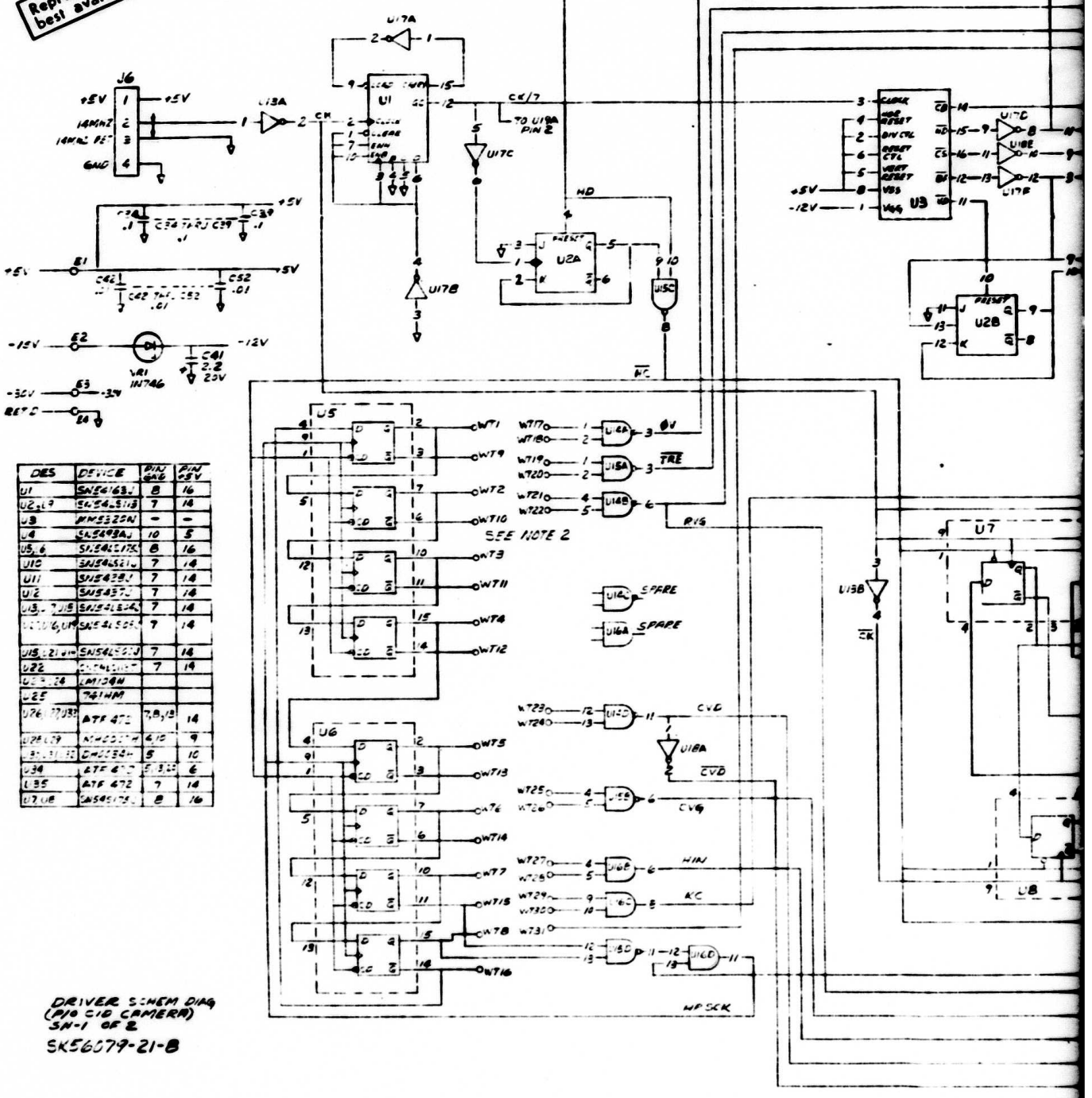


Figure 4-2. Sensor Schematic Diagram (SK56079-21-7)



DES	DEVICE	PIN GND	PIN +5V
U1	SN54163J	8	16
U2,9	SN54LS113	7	14
U3	MM5322N	-	-
U4	SN5409AJ	10	5
U5,6	SN54LS175	8	16
U10	SN54S51J	7	14
U11	SN54S38J	7	14
U12	SN54S37J	7	14
U13, 7,18	SN54LS04J	7	14
U14,16,17	SN54LS00J	7	14
U15,21	SN54LS20J	7	14
U22	SN74LS10J	7	14
U23,24	AM1808N		
U25	74LHM		
U26,27,30	ATF 472	7,8,19	14
U28,29	MM6321N	4,10	9
U31,32	DM8578N	5	10
U34	ATF 472	5,8,12	6
U35	ATF 472	7	14
U7,U8	SN54S175J	8	16

DRIVER SCHEM DIAG (P/O C10 CAMERA) SN-1 OF 2

SK56079-21-B

A

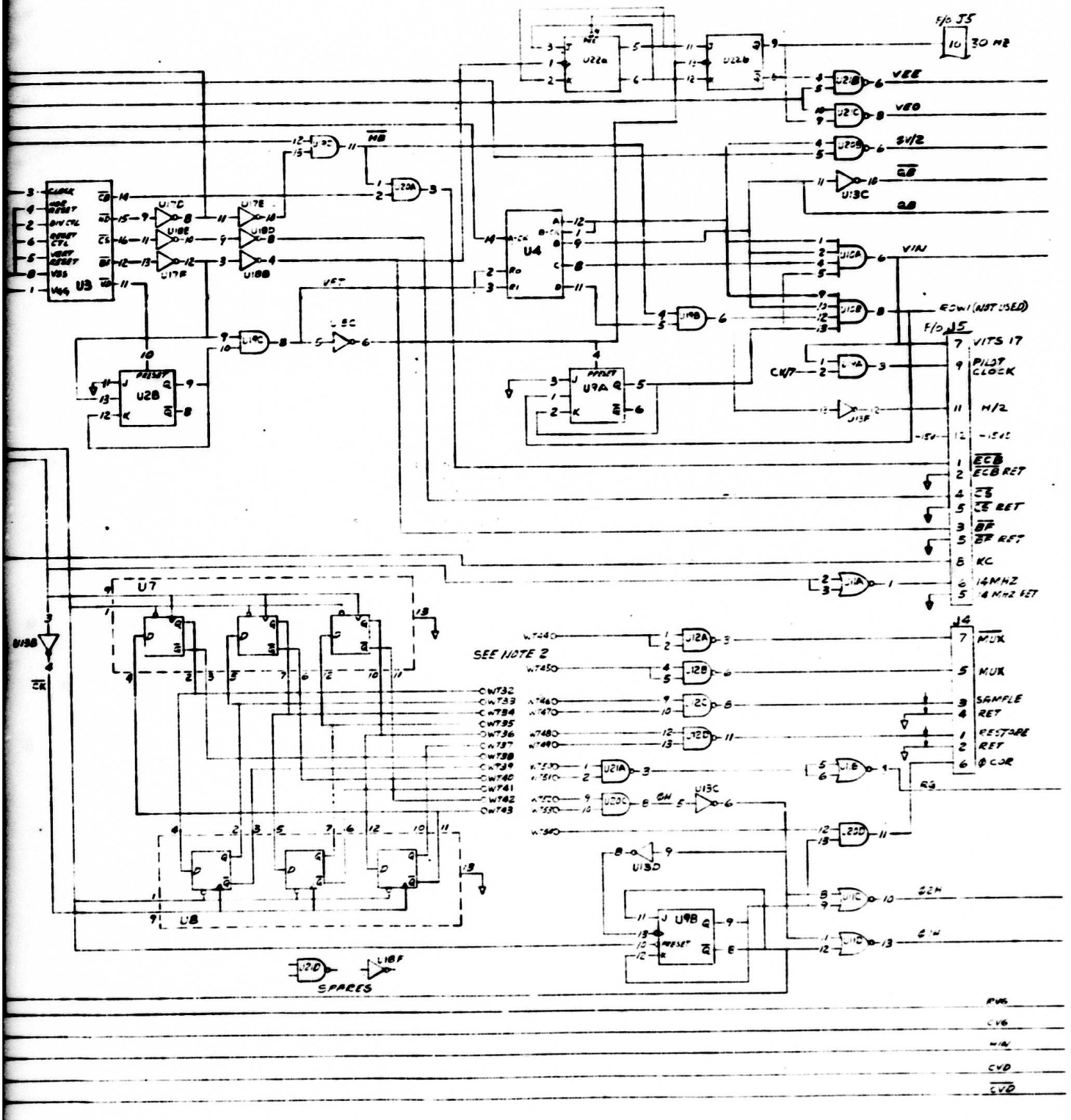
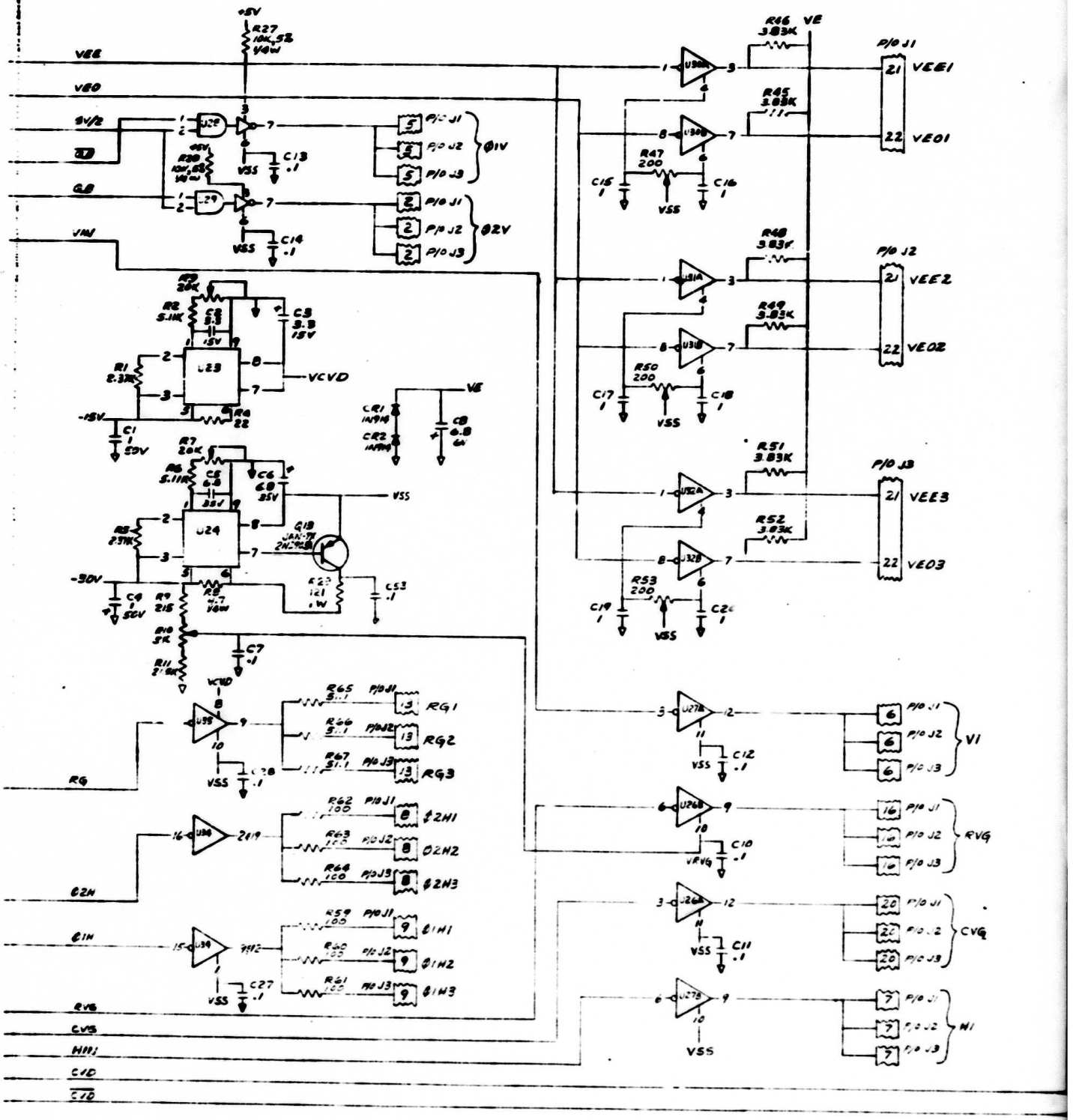


Figure 4-3. Driver Schematic Diagram (SK56079-21-8) (Sheet 1) 4-4


+5V
VEE
VEO
5V/2
GND
G1
G2
VIN
R27 10K 5% 1/4W
U29
U29
R28 10K 5% 1/4W
C13 .1
C14 .1
VSS
P/O J1
P/O J2
P/O J3
Ø1V
Ø2V
R1 2.37K
R2 5.11K
R3 20K
C1 1 50V
C2 6.8 25V
C3 3.3 15V
U23
-15V
VCVD
R4 22
R5 5.11K
R6 2.37K
R7 20K
C5 6.8 35V
C6 68 25V
U24
-30V
C9 1 50V
R8 4.7 1/4W
R9 215
R10 5K
R11 2.15K
C7 .1
Q1B JAN-TX 2N2928
R23 121 1W
C53 .1
CR1 1N914
CR2 1N914
VE
C8 6.8 6V
R46 3.83K
R45 3.83K
R47 200
C15 1
C16 1
U30A
U30B
P/O J1
21
22
VEE1
VEO1
R48 3.83K
R49 3.83K
R50 200
C17 1
C18 1
U31A
U31B
P/O J2
VEE2
VEO2
R51 3.83K
R52 3.83K
R53 200
C19 1
C20 1
U32A
U32B
P/O J3
VEE3
VEO3
U39
U39
U39
R65 51.1
R66 51.1
R67 51.1
R62 100
R63 100
R64 100
R59 100
R60 100
R61 100
C28 .1
C27 .1
RG1
RG2
RG3
Ø2H1
Ø2H2
Ø2H3
Ø1H1
Ø1H2
Ø1H3
RG
Ø2H
Ø1H
RVG
CVG
H111
C1D
C1D
U27A
U26B
U26A
U27B
C12 .1
C10 .1
C11 .1
VRVG
VI
RVG
CVG
H1
P/O J1
P/O J2
P/O J3

A

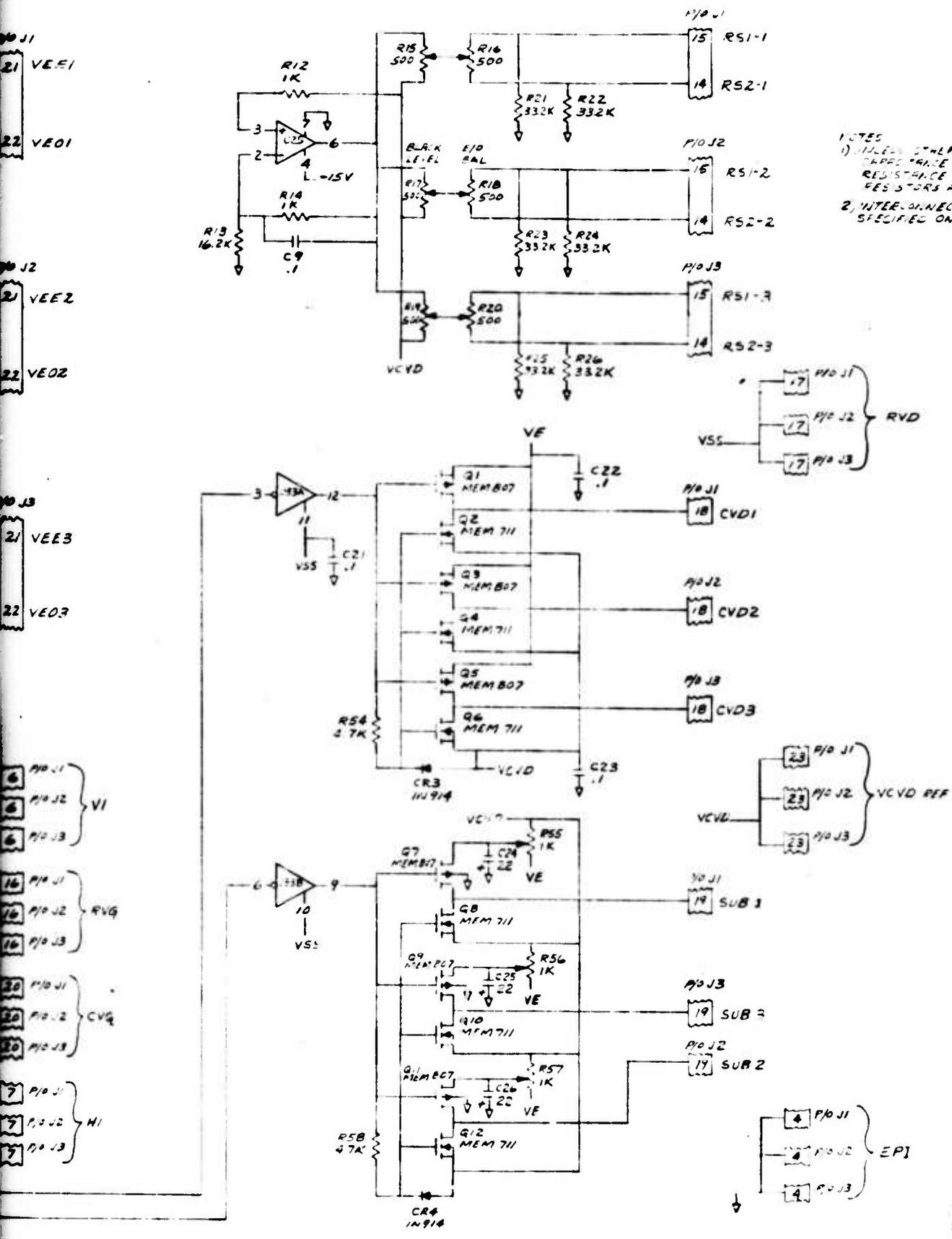


Figure 4-3. Driver Schematic Diagram (SK56079-21-8) (Sheet 2)

INJECTION TIMING

FUNCTION		CLOCK*	CONNECTION	
ϕV	START	13	WT17	WT13
	STOP	14	WT18	WT 6
TRE	START	6	WT19	WT6
	STOP	14	WT20	WT 6
RVG	START	6	WT21	WT6
	STOP	7	WT22	WT15
CVD	START	1	WT23	WT1
	STOP	6	WT24	WT14
CVG	START	1	WT25	WT9
	STOP	12	WT26	WT12
HIN	START	14	WT27	WT14
	STOP	15	WT28	WT7
KC	START	8	WT29	WT8
	STOP	12	WT30	WT4
HB	START	1	—	—
	STOP	15	WT31	WT15

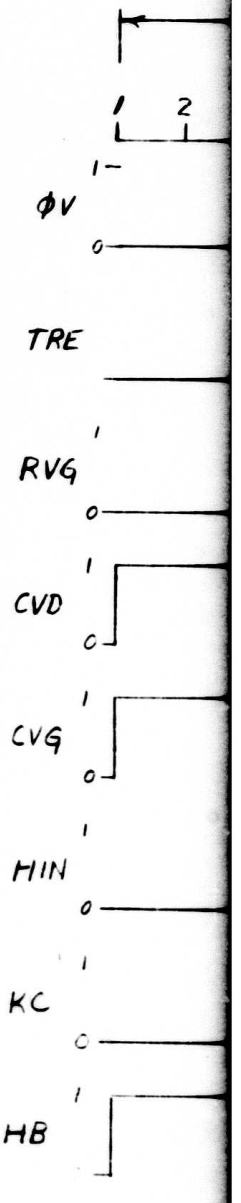
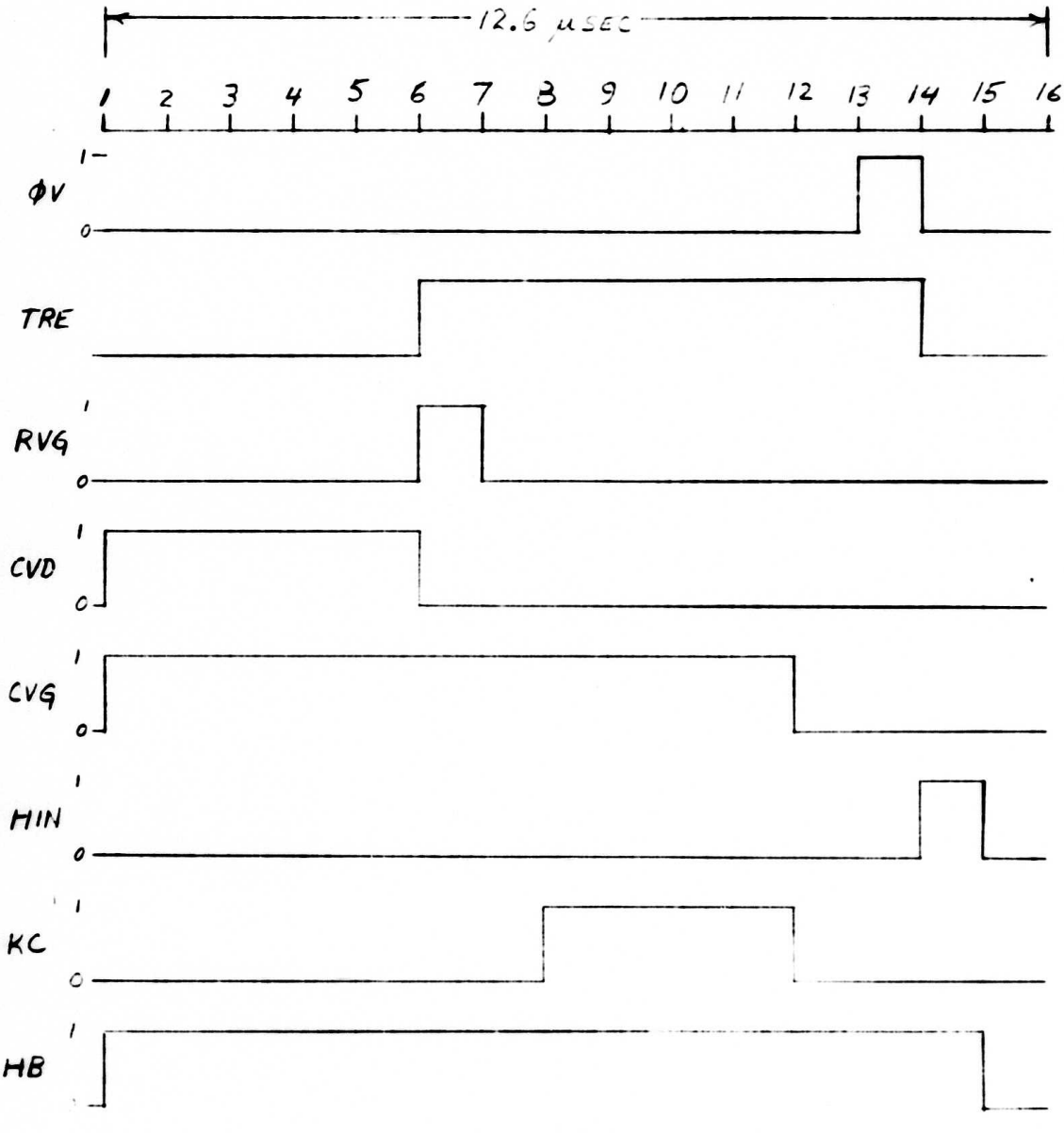


Figure 4-4. Timing Interce

A



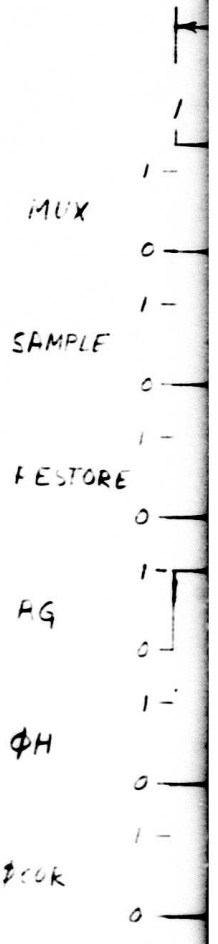
TIMING INTERCONNECTION TABLE

SK56079-21-26
SHEET 1 OF 2

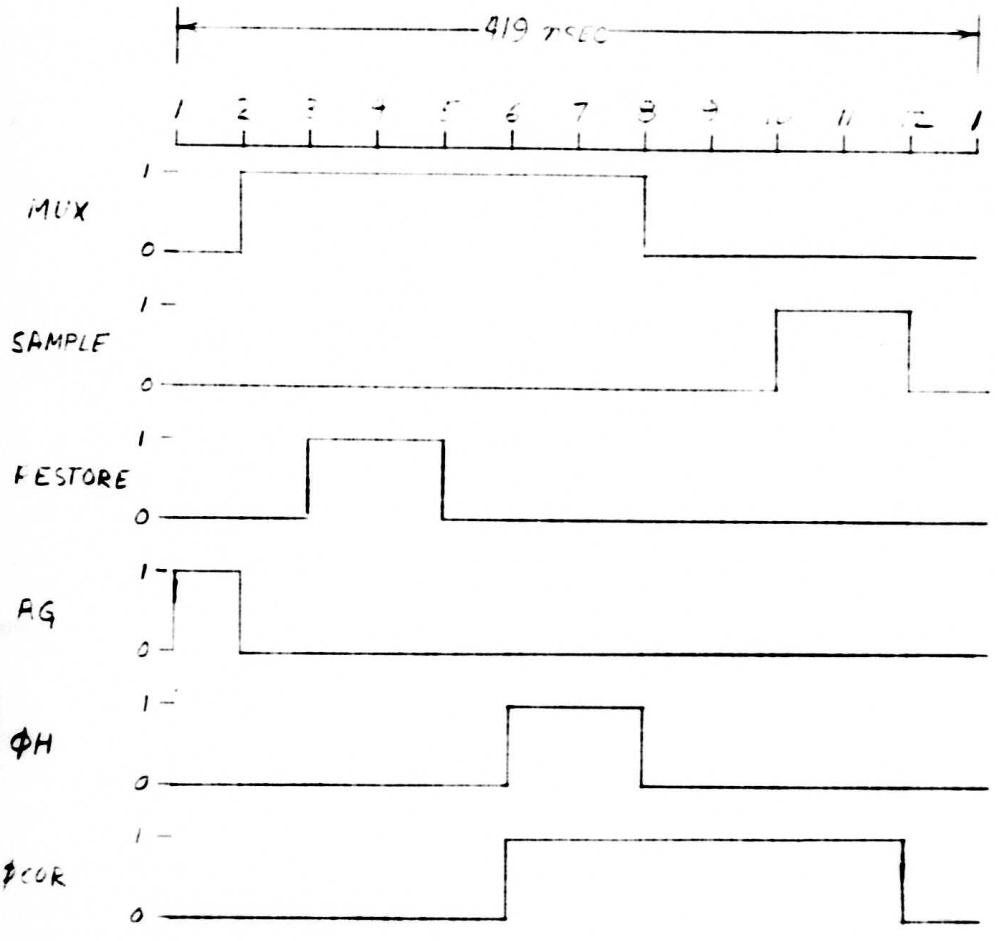
e 4-4. Timing Interconnection Table (SK56079-21-26) (Sheet 1)

ELEMENT [illegible]

FUNCTION		CLOCK #	CONNECTION	
MUX		2	WT44	WT39
$\overline{MUX}$		8	WT45	WT33
SAMPLE	START	10	WT46	WT41
	STOP	12	WT47	WT37
RESTORE	START	3	WT48	WT34
	STOP	5	WT49	WT42
RG	START	1	WT50	WT32
	STOP	2	WT51	WT39
ϕH	START	6	WT52	WT37
	STOP	8	WT53	WT33
ϕCOR (OLD ELEMENTS ONLY)		6	WT54	WT37



A



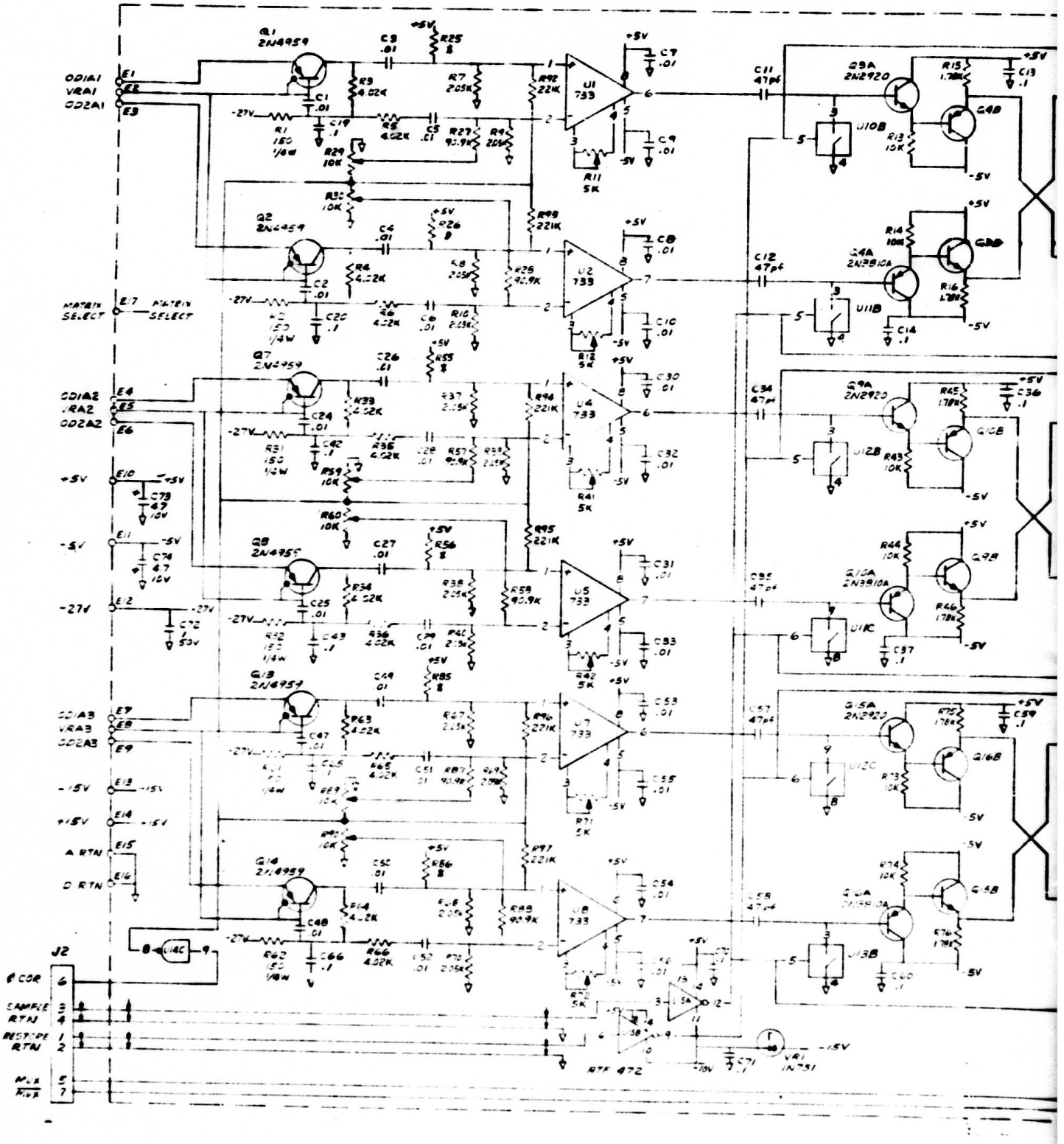
TIMING INTERCONNECTION TABLE

SK56079-21-26

SHEET 2 OF 2

Figure 4-4. Timing Interconnection Table (SK56079-21-26) (Sheet 2)

B


ODIA1
VRA1
ODZA1
E1
E2
E3
Q1 2N4959
C9 .01
+5V
R25 8
R3 4.02K
R7 205K
R92 221K
U1 733
C7 .01
C11 47pf
Q9A 2N2920
R15 1.78K
C13 .1
U10B
R13 10K
Q4B
-5V
C1 .01
C19 .1
R1 150 1/4W
-27V
R5 4.02K
C5 .01
R27 92.9K
R91 205K
R29 10K
R11 5K
R32 10K
Q2 2N4959
C4 .01
R26 8
R4 4.02K
R8 205K
R26 92.9K
R99 221K
U2 733
C8 .01
C12 47pf
Q4A 2N3810A
R14 10K
Q3B
R16 1.78K
U11B
C14 .1
C2 .01
C20 .1
R2 150 1/4W
R6 4.02K
C6 .01
R16 205K
R12 5K
C10 .01
MATRIX SELECT
E7
Q7 2N4959
C26 .01
R55 8
R33 4.02K
R37 205K
R94 221K
U4 733
C30 .01
C34 47pf
Q9A 2N2920
R45 1.78K
C36 .1
Q10B
U12B
R43 10K
C24 .01
C42 .1
R51 150 1/4W
R36 4.02K
C28 .01
R57 92.9K
R93 205K
R39 10K
R41 5K
C32 .01
ODIA2
VRA2
ODZA2
E4
E5
E6
+5V
E10
C73 47 10V
-5V
E11
C74 47 10V
-27V
E12
C72 1 50V
Q8 2N4959
C27 .01
R56 8
R34 4.02K
R38 205K
R98 92.9K
U5 733
C31 .01
C35 47pf
Q9A 2N2920
R44 10K
Q9B
Q11A 2N3810A
R46 1.78K
U11C
C37 .1
R42 5K
C33 .01
R32 150 1/4W
R36 4.02K
C29 .01
R40 205K
Q13 2N4959
C49 .01
R85 8
R63 4.02K
R67 205K
R96 221K
U7 733
C53 .01
C57 47pf
Q15A 2N2920
R75 1.78K
C59 .1
Q16B
U13C
R73 10K
C47 .01
C45 .1
R65 4.02K
C51 .01
R87 92.9K
R69 205K
R89 10K
R71 5K
C55 .01
ODIA3
VRA3
ODZA3
E7
E8
E9
-15V
E13
+15V
E14
A RTN
E15
D RTN
E16
R97 10K
R97 221K
C50 .01
R66 8
R64 4.02K
R68 205K
R88 92.9K
U8 733
C54 .01
C58 47pf
Q14 2N4959
Q16A 2N3810A
Q15B
R74 10K
R76 1.78K
U13B
C60 .1
R72 5K
C56 .01
R62 150 1/4W
R66 4.02K
C52 .01
R70 205K
J2
Ø COR
SAMPLE RTN
RESTORE RTN
MUX
MUX RTN
RTF 472
C71 .1
VR1 1N751
-15V

A

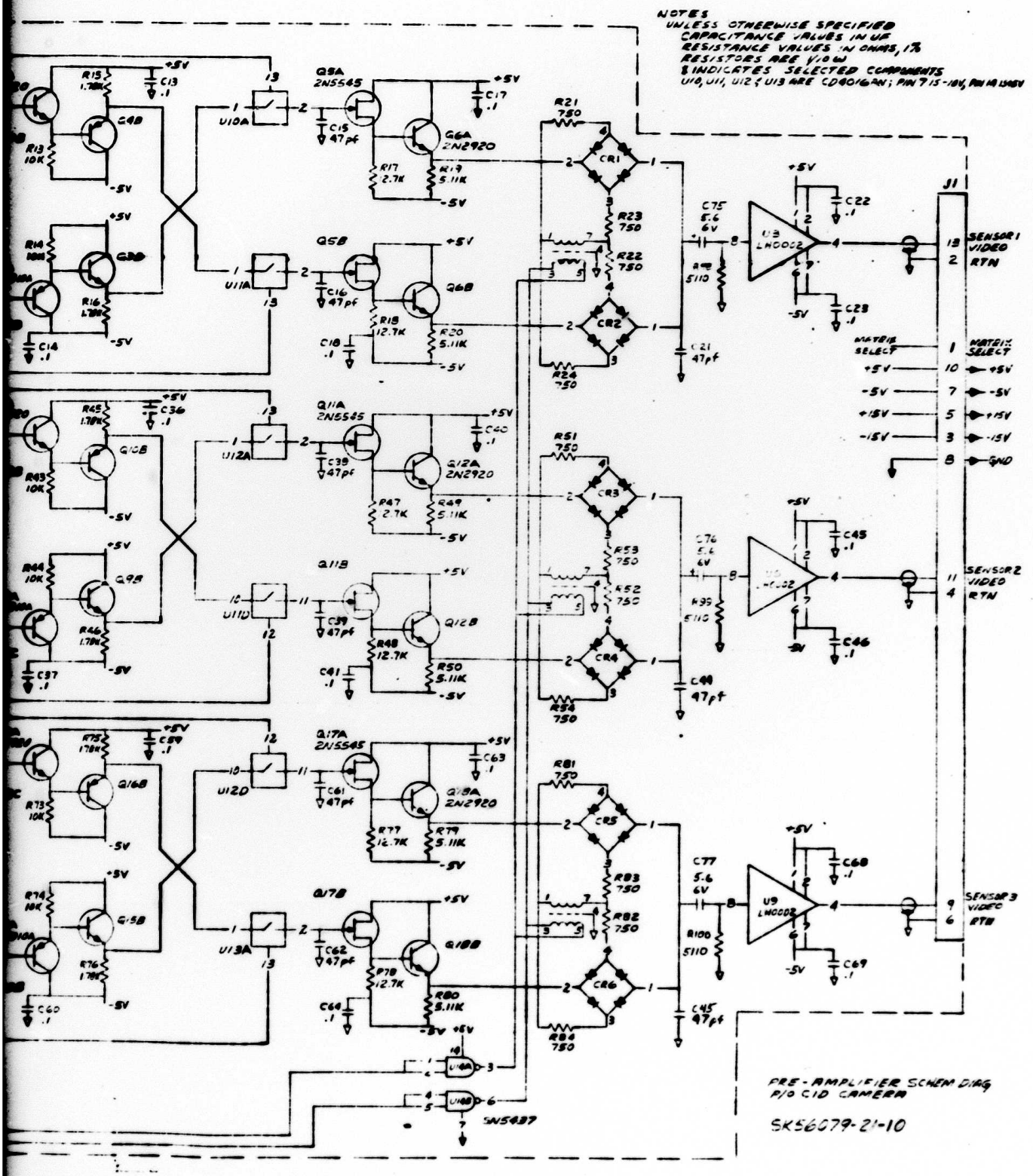
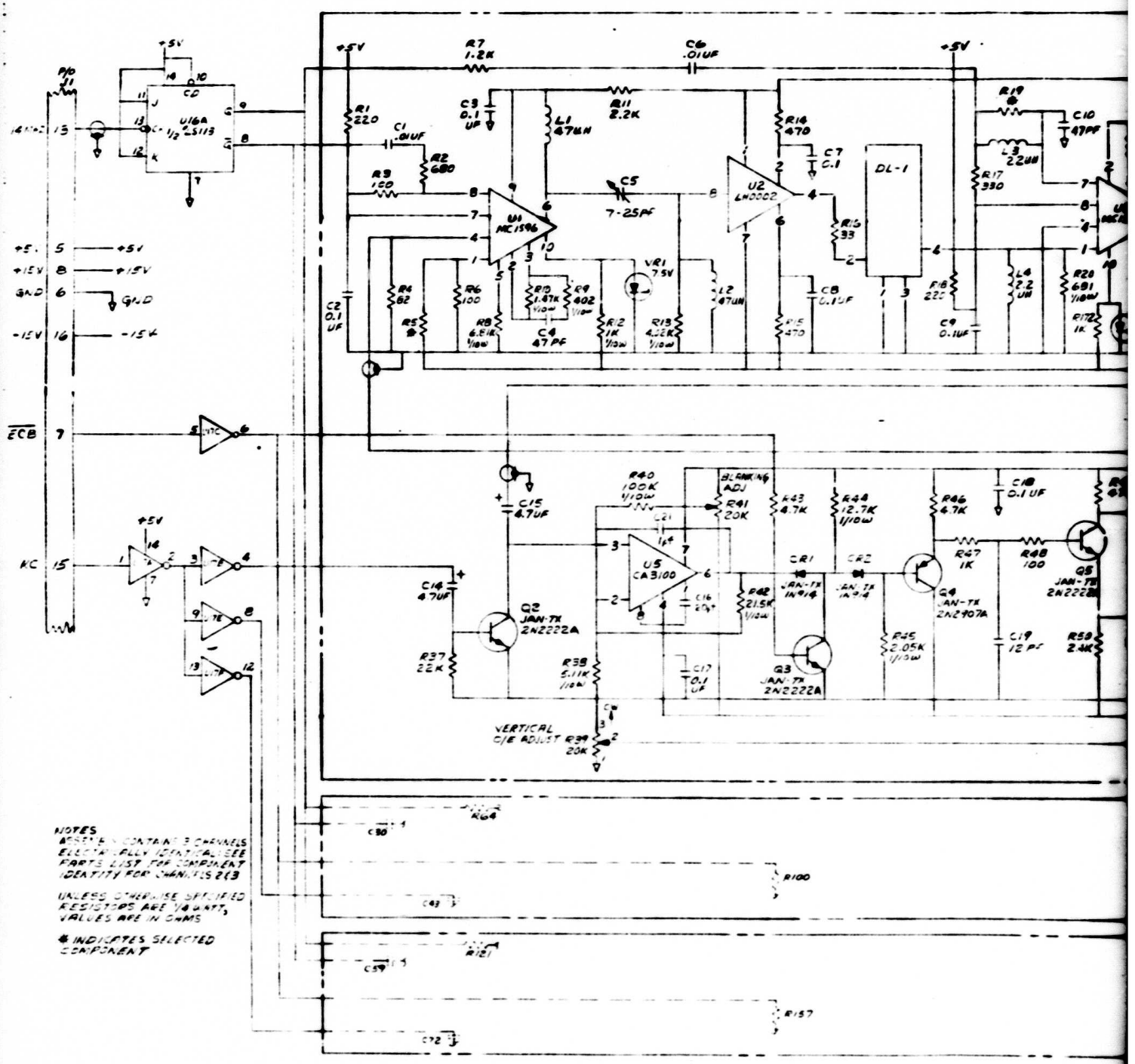


Figure 4-5. Preamplifier Schematic Diagram (SK56079-21-10)



NOTES

A7571-1 CONTAINS 3 CHANNELS ELECTRICALLY IDENTICAL SEE PARTS LIST FOR COMPONENT IDENTITY FOR CHANNELS 2 & 3

UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4 WATT, VALUES ARE IN OHMS

* INDICATES SELECTED COMPONENT

A

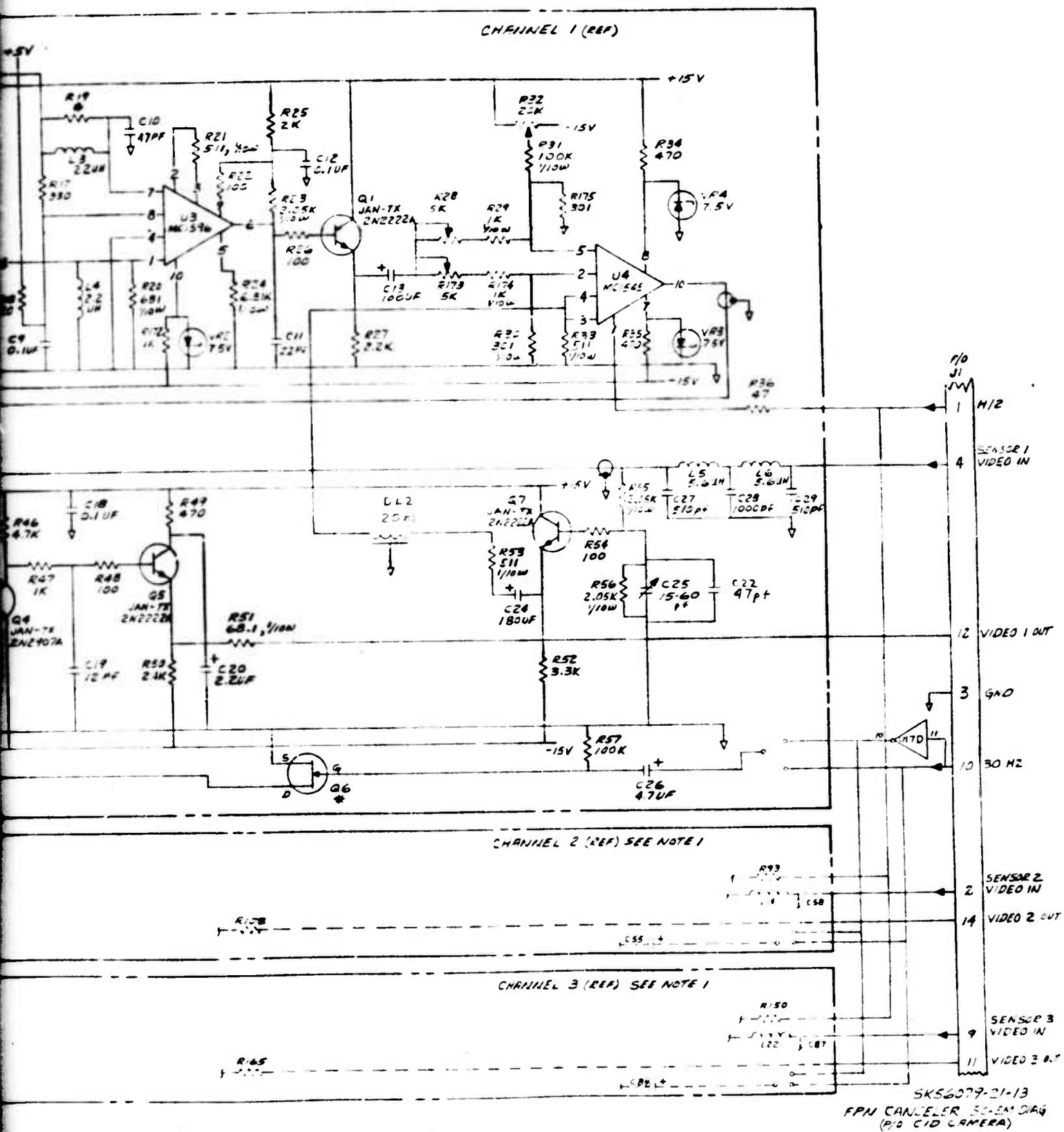
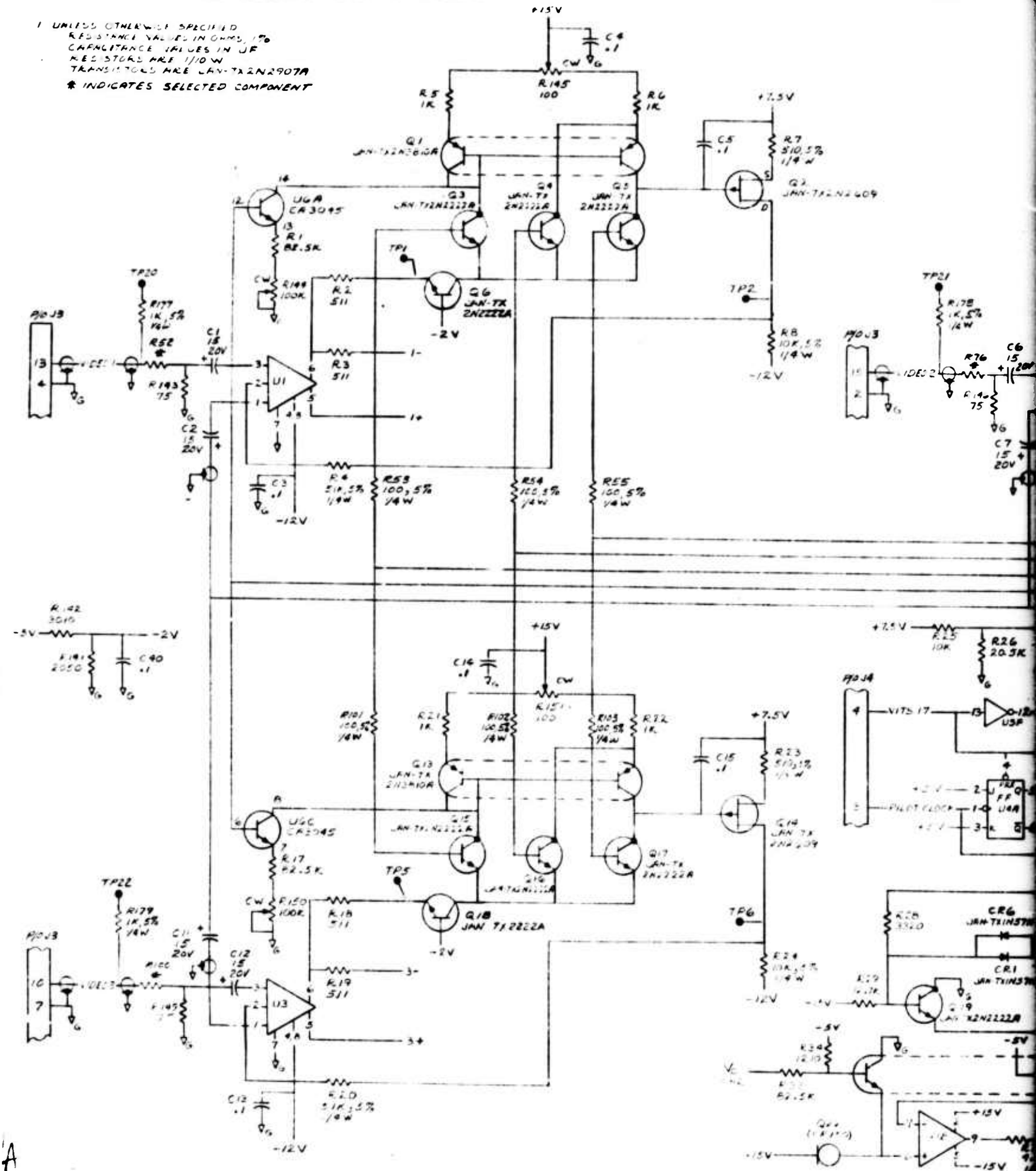


Figure 4-6. FPN Canceler Schematic Diagram (SK56079-21-13)

1. UNLESS OTHERWISE SPECIFIED
   RESISTANCE VALUES IN OHMS, 1%
   CAPACITANCE VALUES IN UF
   RESISTORS ARE 1/10 W
   TRANSISTORS ARE JAN-TX2N2907A
   * INDICATES SELECTED COMPONENT



A

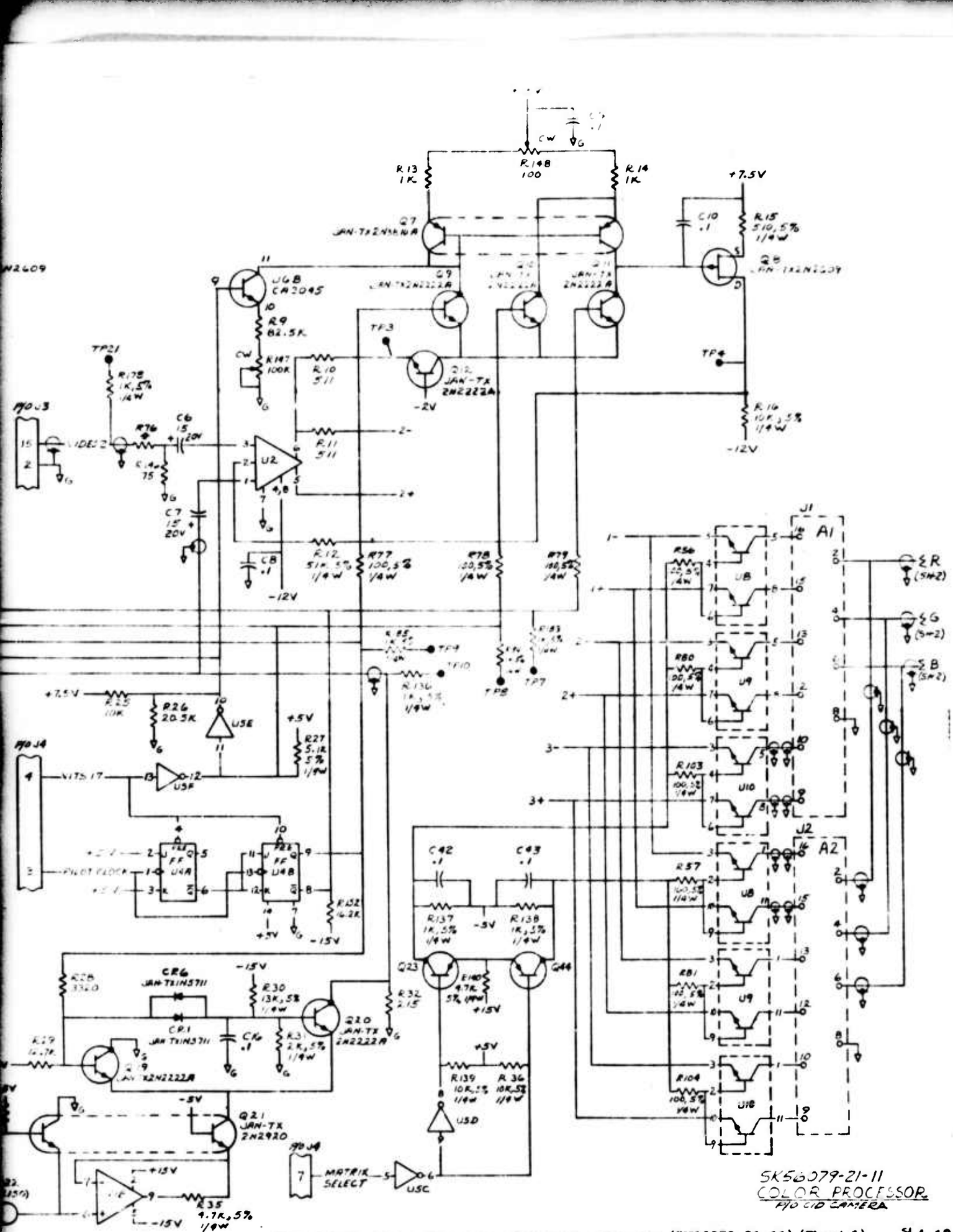
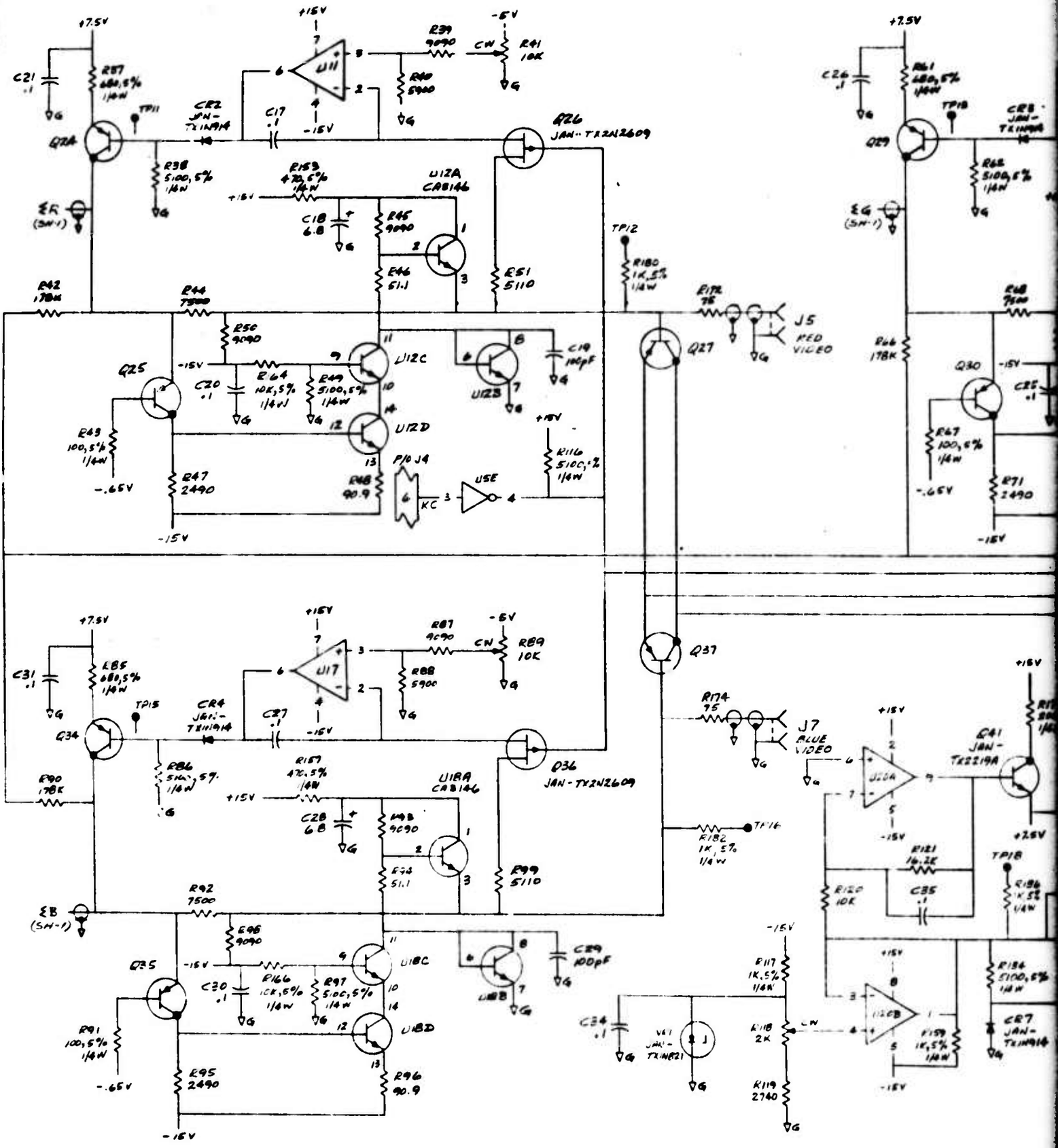


Figure 4-7. Color Processor Schematic Diagram (SK56079-21-11) (Sheet 1) 4-10


+7.5V
C21 .1
R37 680, 5% 1/4W
TP11
Q2A
CR2 JAN-TX1N914
C17 .1
+15V
U11
-15V
R39 9090
CW
R41 10K
-5V
R40 5900
Q26 JAN-TX2N2609
R38 5100, 5% 1/4W
ER (SW-1)
R153 470, 5% 1/4W
U12A CA3146
C18 6.8
R45 9090
R46 51.1
R51 5110
TP12
R180 1K, 5% 1/4W
R42 178K
R44 7500
R56 9090
Q25
C20 .1
R64 10K, 5% 1/4W
R49 5100, 5% 1/4W
U12C
U12B
C19 100pF
U12D
R43 100, 5% 1/4W
-.65V
R47 2490
P/O J4
R48 90.9
KC
USE
R116 5100, 5% 1/4W
Q27
R178 75
J5 RED VIDEO
+7.5V
C24 .1
R61 680, 5% 1/4W
TP13
CR8 JAN-TX1N914
Q29
R62 5100, 5% 1/4W
EG (SW-1)
R48 7500
R66 178K
Q30
C25 .1
R67 100, 5% 1/4W
-.65V
R71 2490
-15V
+7.5V
C31 .1
R85 680, 5% 1/4W
TP15
CR4 JAN-TX1N914
Q34
C27 .1
+15V
U17
-15V
R87 9090
CW
R89 10K
-5V
R88 5900
Q37
R174 75
J7 BLUE VIDEO
Q36 JAN-TX2N2609
R86 5K, 5% 1/4W
R90 178K
R157 470, 5% 1/4W
U18A CA3146
C28 6.8
R93 9090
R94 51.1
R99 5110
R182 1K, 5% 1/4W
TP16
EB (SW-1)
R92 7500
R98 9090
Q35
C30 .1
R166 10K, 5% 1/4W
R97 5100, 5% 1/4W
U18C
U18B
C29 100pF
U18D
R91 100, 5% 1/4W
-.65V
R95 2490
R96 90.9
+15V
U20A
Q41 JAN-TX2219A
R121 16.2K
R120 10K
C35 .1
TP18
R184 1K, 5% 1/4W
R184 5100, 5% 1/4W
CR7 JAN-TX1N914
U20B
R117 1K, 5% 1/4W
R159 1K, 5% 1/4W
C34 .1
V41 JAN-TX1N821
R118 2K
R119 2740

A

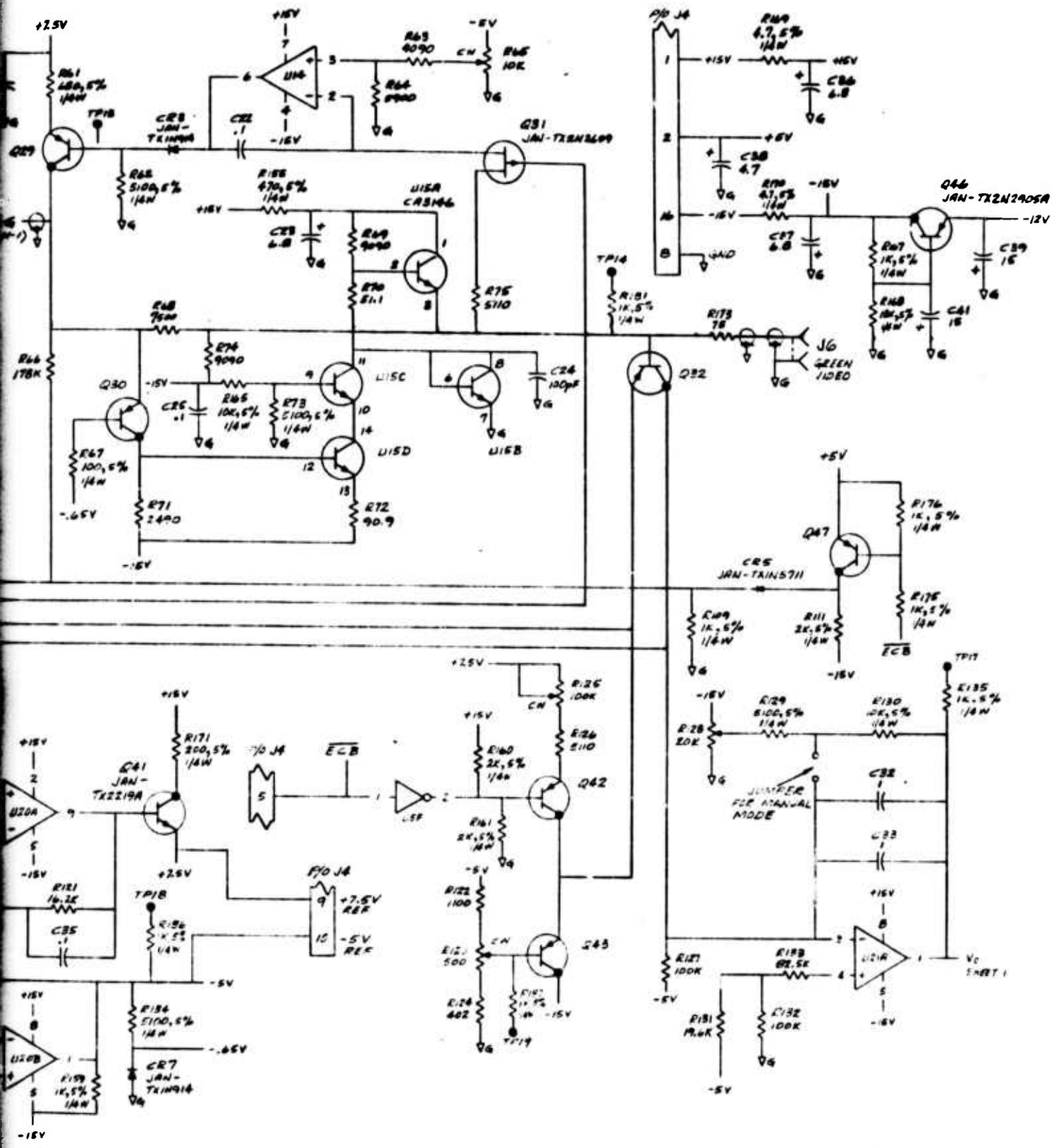
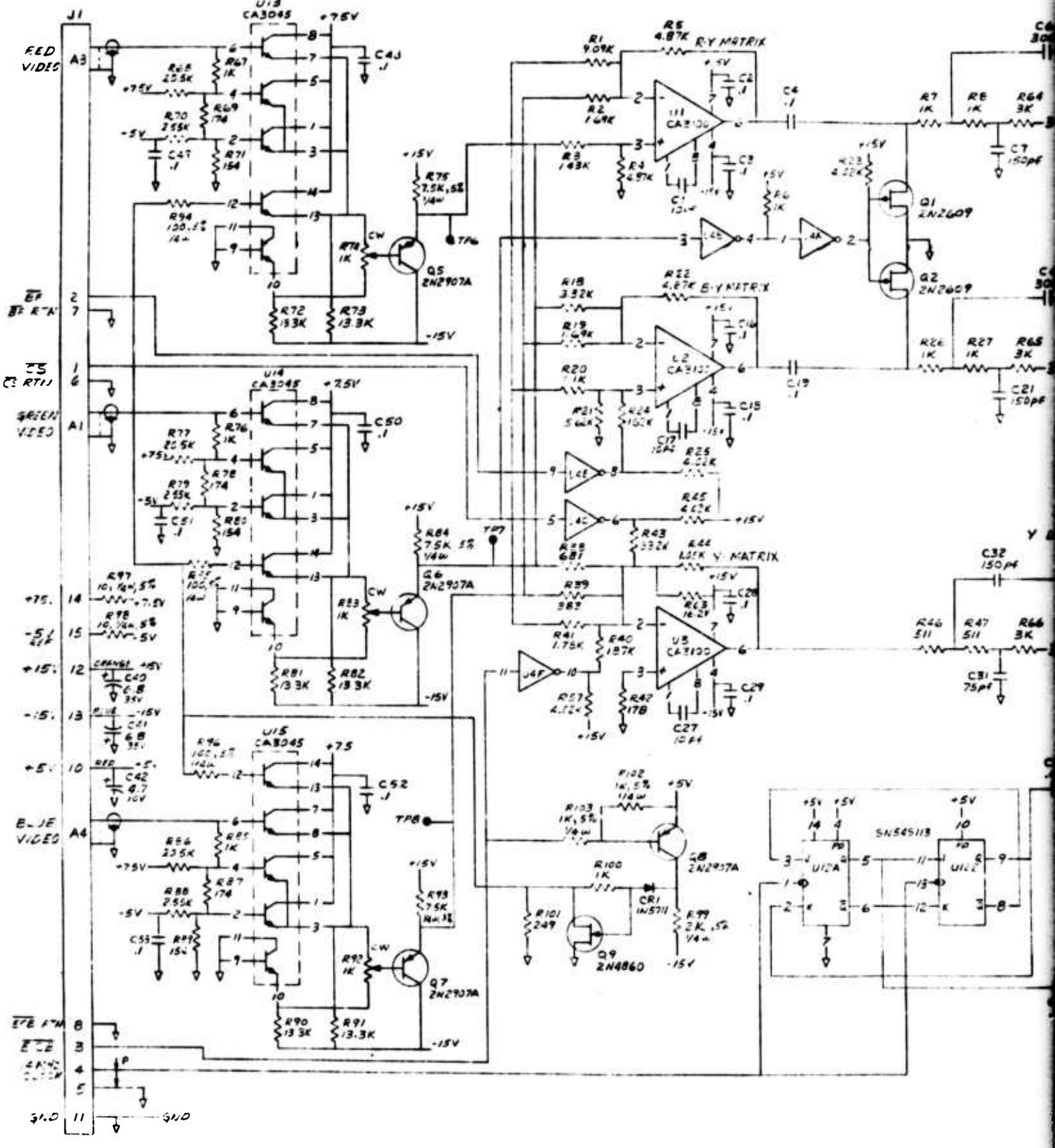


Figure 4-7. Color Processor Schematic Diagram (SK56079-21-11) (Sheet 2)


J1
RED VIDEO
A3
GREEN VIDEO
A1
BLUE VIDEO
A4
+7.5V
-5V
+15V
-15V
+5V
GND
U13 CA3045
U14 CA3045
U15 CA3045
R-Y MATRIX
B-Y MATRIX
LUM Y MATRIX
U1 CA3100
U2 CA3100
U3 CA3100
Q1 2N2609
Q2 2N2609
Q5 2N2907A
Q6 2N2907A
Q7 2N2907A
Q8 2N2907A
Q9 2N4860
CR1 IN5711
SN54S113
U1A
U1B
TP6
TP7
TP8

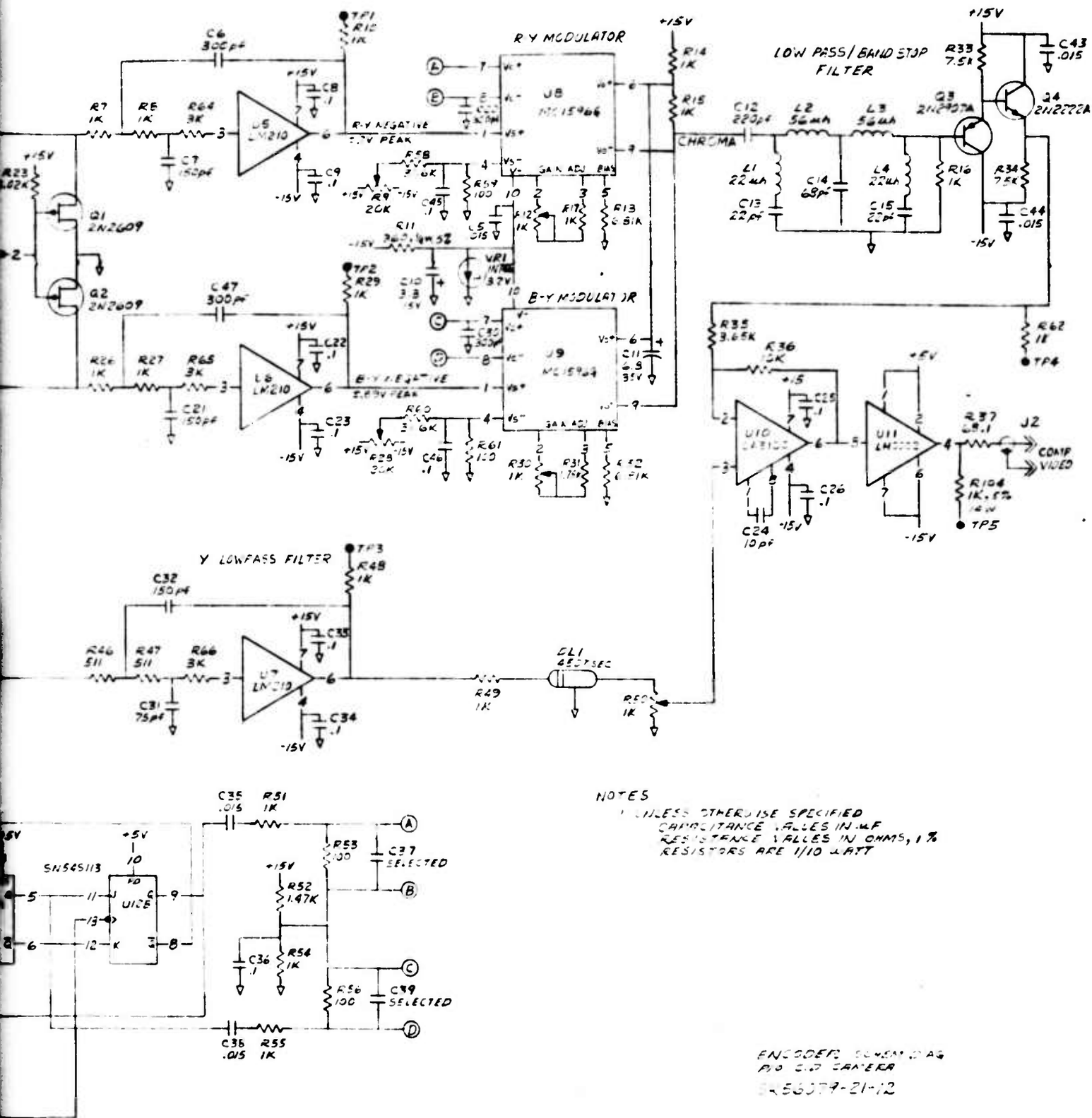
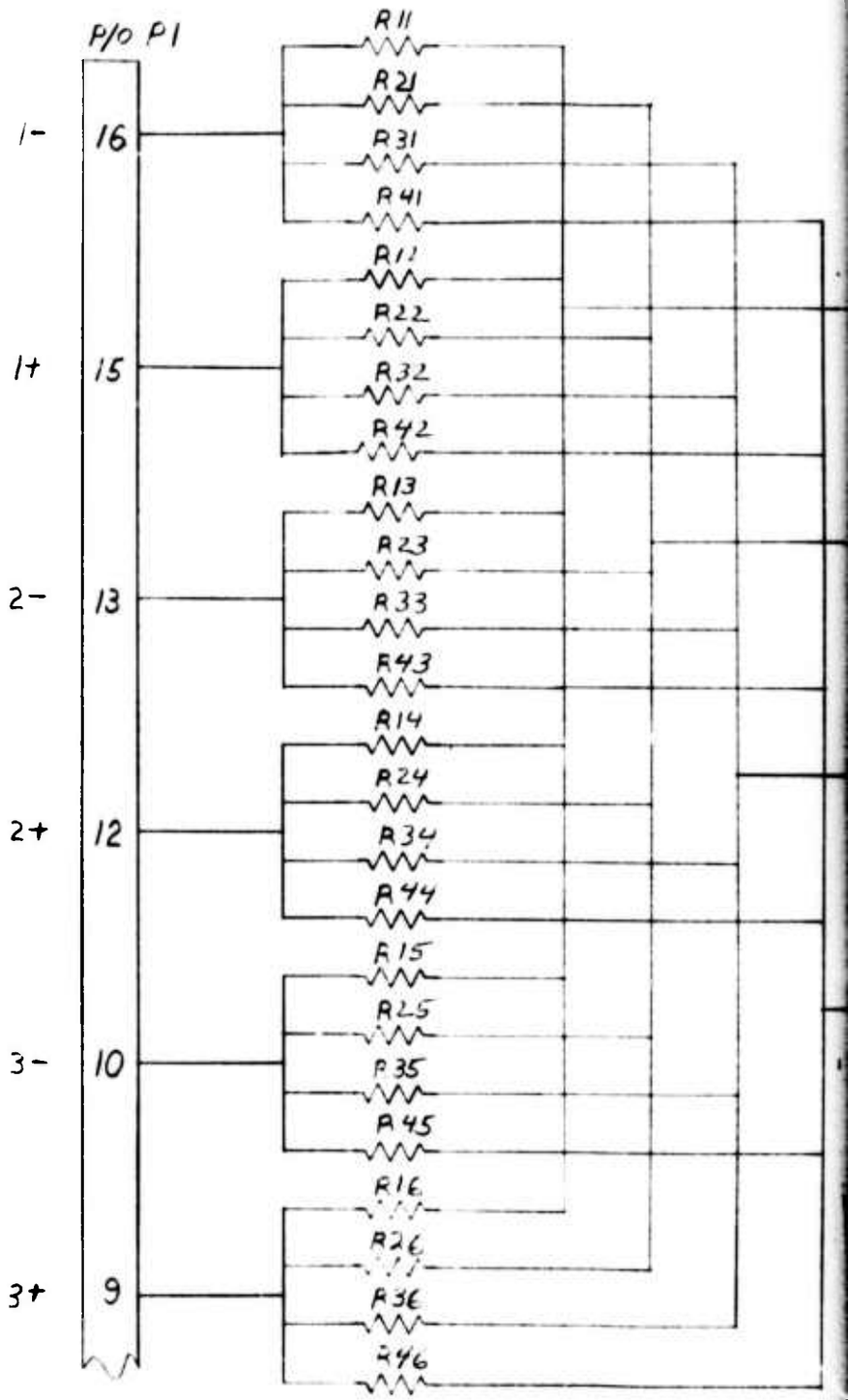
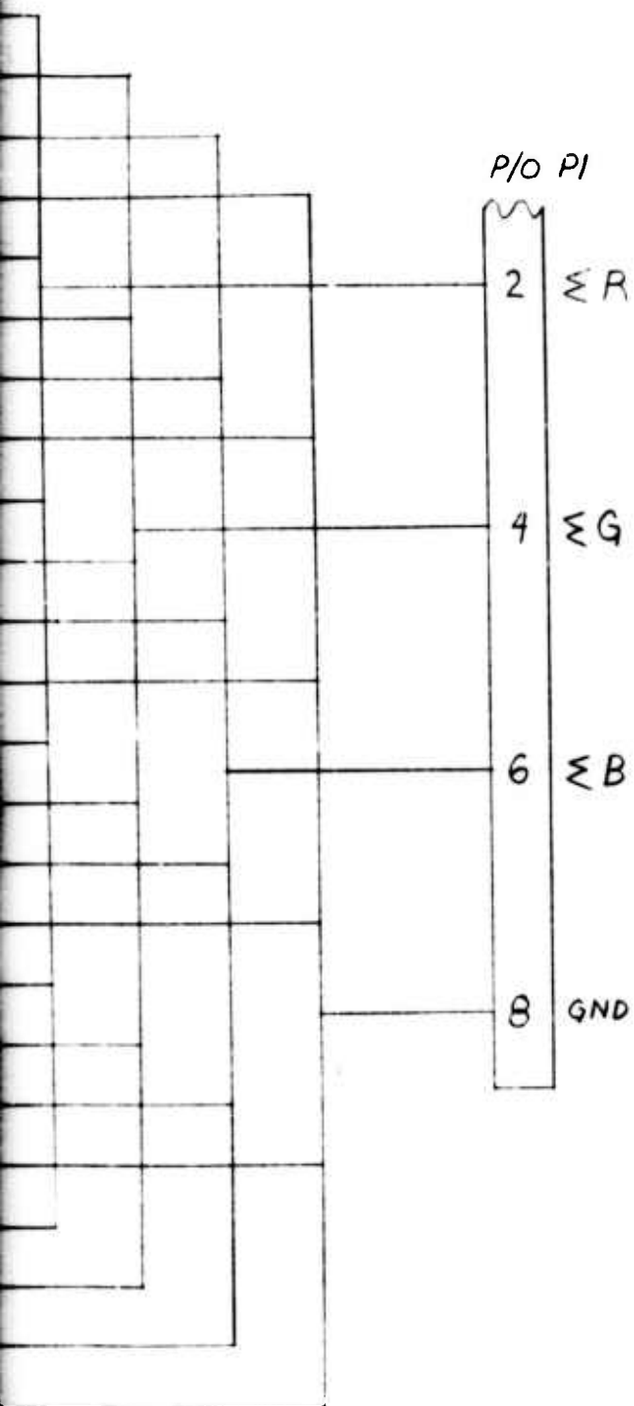


Figure 4-8. Encoder Schematic Diagram (SK56079-21-12)


P/O P1
1-
16
1+
15
2-
13
2+
12
3-
10
3+
9
R11
R21
R31
R41
R12
R22
R32
R42
R13
R23
R33
R43
R14
R24
R34
R44
R15
R25
R35
R45
R16
R26
R36
R46

A



NOTE:
THIS SCHEMATIC IS FOR REFERENCE ONLY, AND REPRESENTS ALL POSSIBLE VALID COMBINATIONS OF RESISTORS AND BUS WIRES TO ACHIEVE ANY PERMISSIBLE SET OF MATRIX COEFFICIENTS

EACH RESISTOR SHOWN MAY ACTUALLY BE ONE OF THE FOLLOWING:

1) A BUS WIRE
2) A RESISTOR, TYPE RNC50H, WITH VALUE BETWEEN 205Ω AND 10K
3) NO COMPONENT OR WIRE I.E. AN OPEN CIRCUIT

THE SPECIFIC DESIGN WILL DEPEND ON THE APPLICATION

PLUG-IN MATRIX

SK56079-21-14

Figure 4-9. Plug-In Matrix Schematic Diagram (SK56079-21-14)

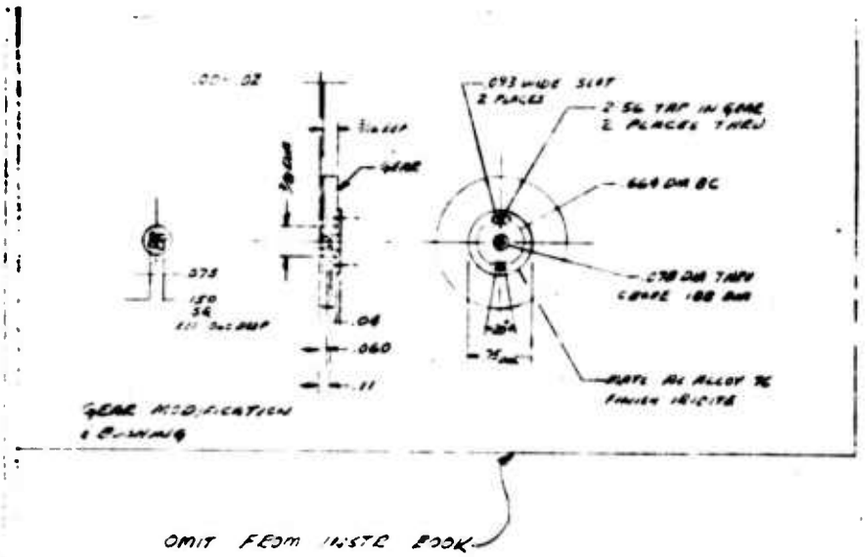
SECTION IV

ASSEMBLY DRAWINGS

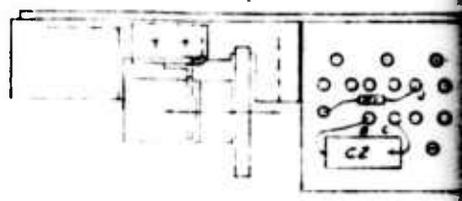
5.1 ORGANIZATION

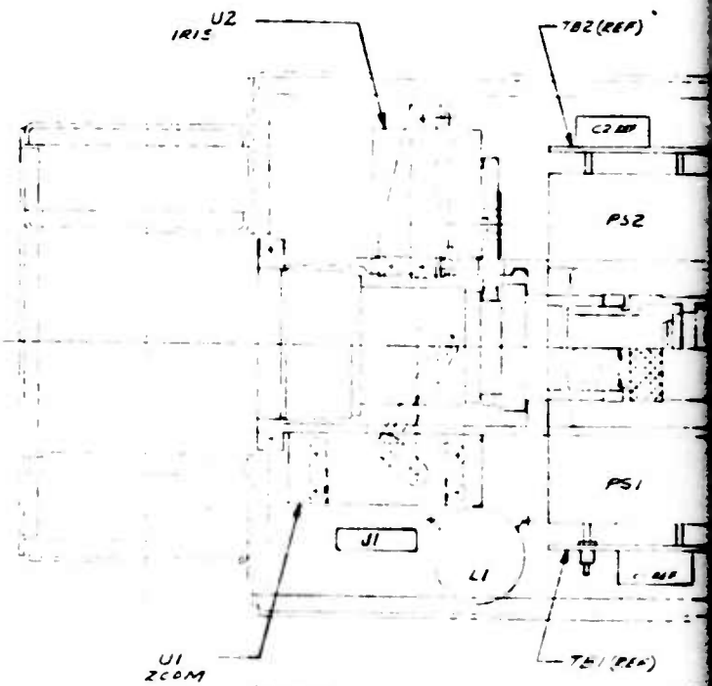
The assembly drawings in this section are arranged in order of the reference designator A1 to A9, preceded by the unit assembly drawing.

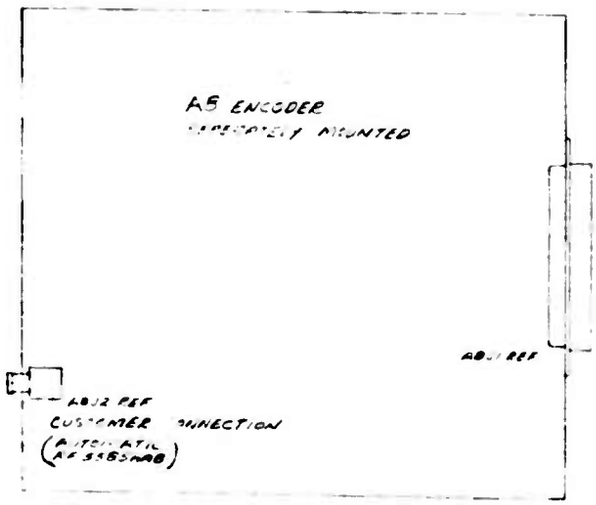
The Assembly drawings are cross-referenced to the schematic diagrams and the theory of operation by Table 2-1.



OMIT FROM INSTR BOOK







A

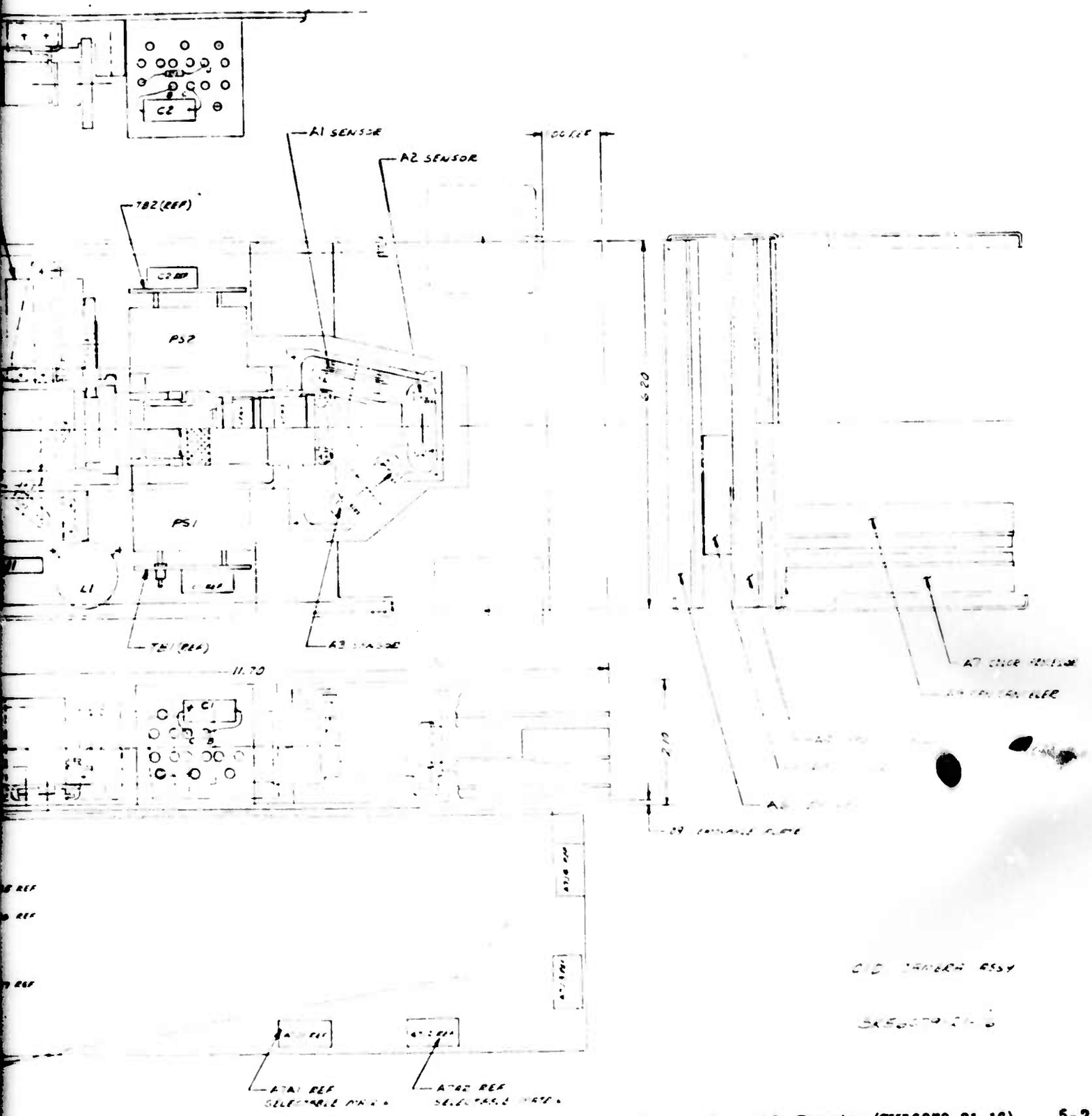


Figure 5-1. CID Camera Assembly Drawing (SK56079-21-16)

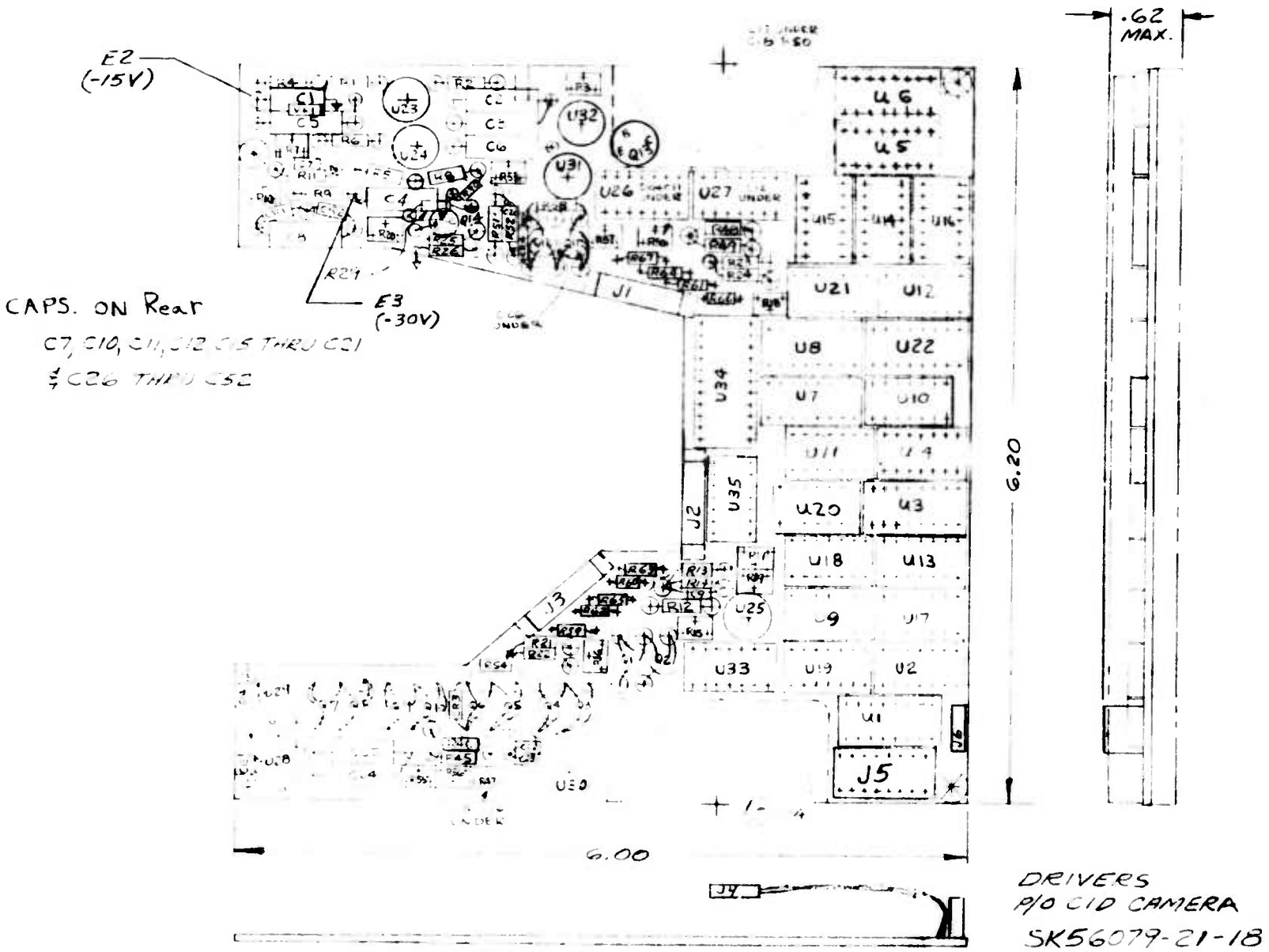
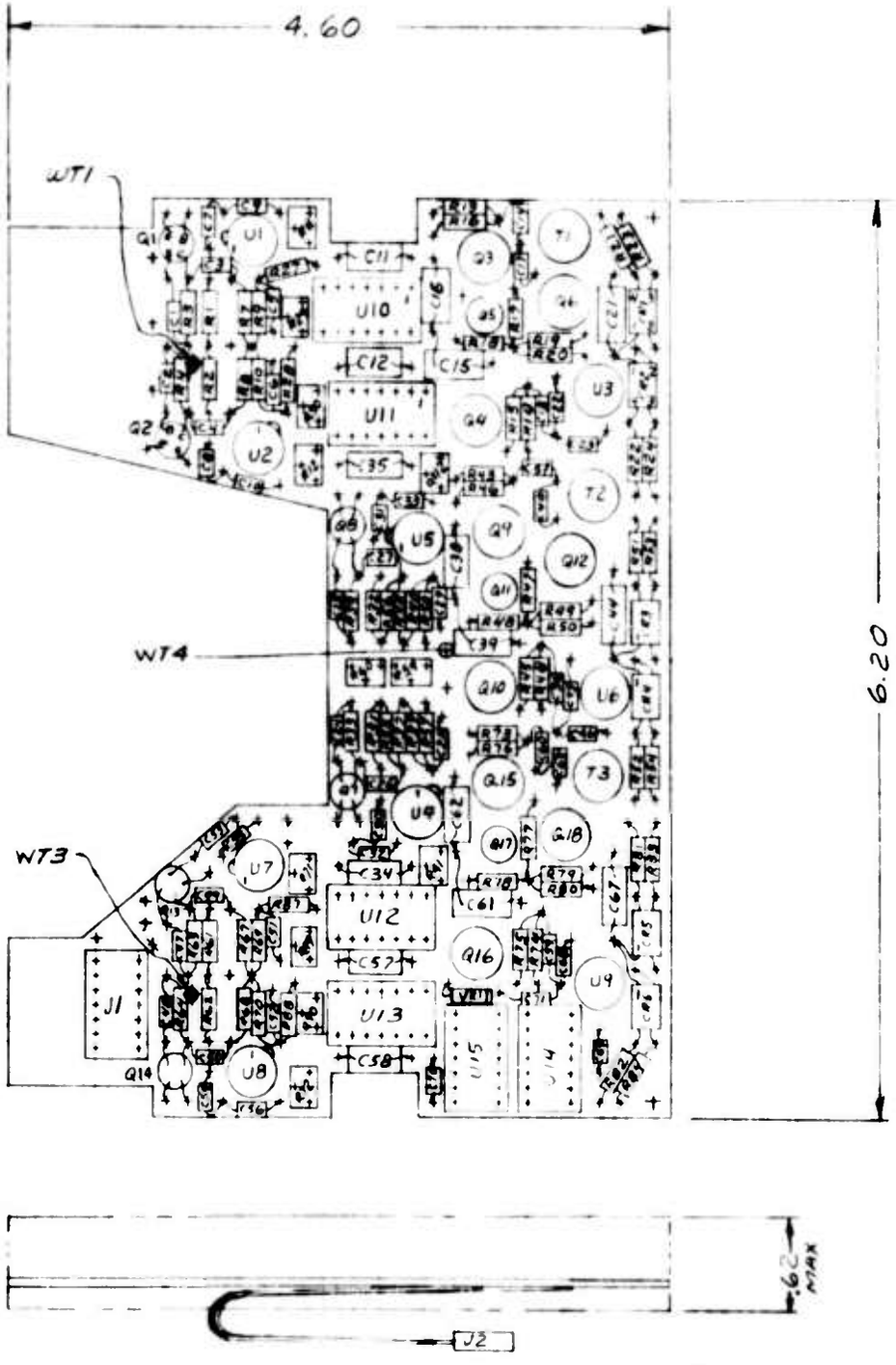
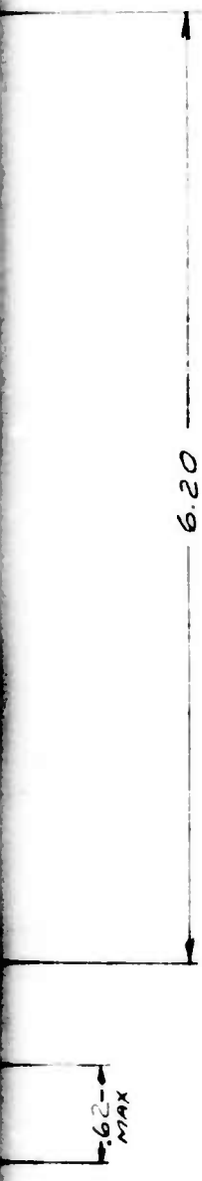
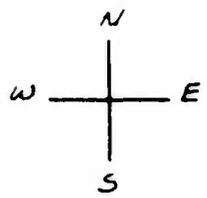


Figure 5-2. Driver Assembly Drawing (SK56079-21-18)


4.60
WT1
WT4
WT3
J1
J2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
T1
T2
T3
Q1
Q2
Q3
Q4
Q5
Q6
Q9
Q10
Q11
Q12
Q15
Q16
Q17
Q18
C11
C12
C15
C35
C39
C34
C61
C57
C58
.62
MAX



COMPONENTS NOT DELINEATED FOR CLARITY



COMPONENTS LOCATED ON FS

	FROM	TO
R5	R3-S	C5-S
R6	R4-N	C6-N
R35	R33-N	C28-N
R36	R34-S	C29-S
R65	R63-S	C51-S
R66	R64-N	C52-N

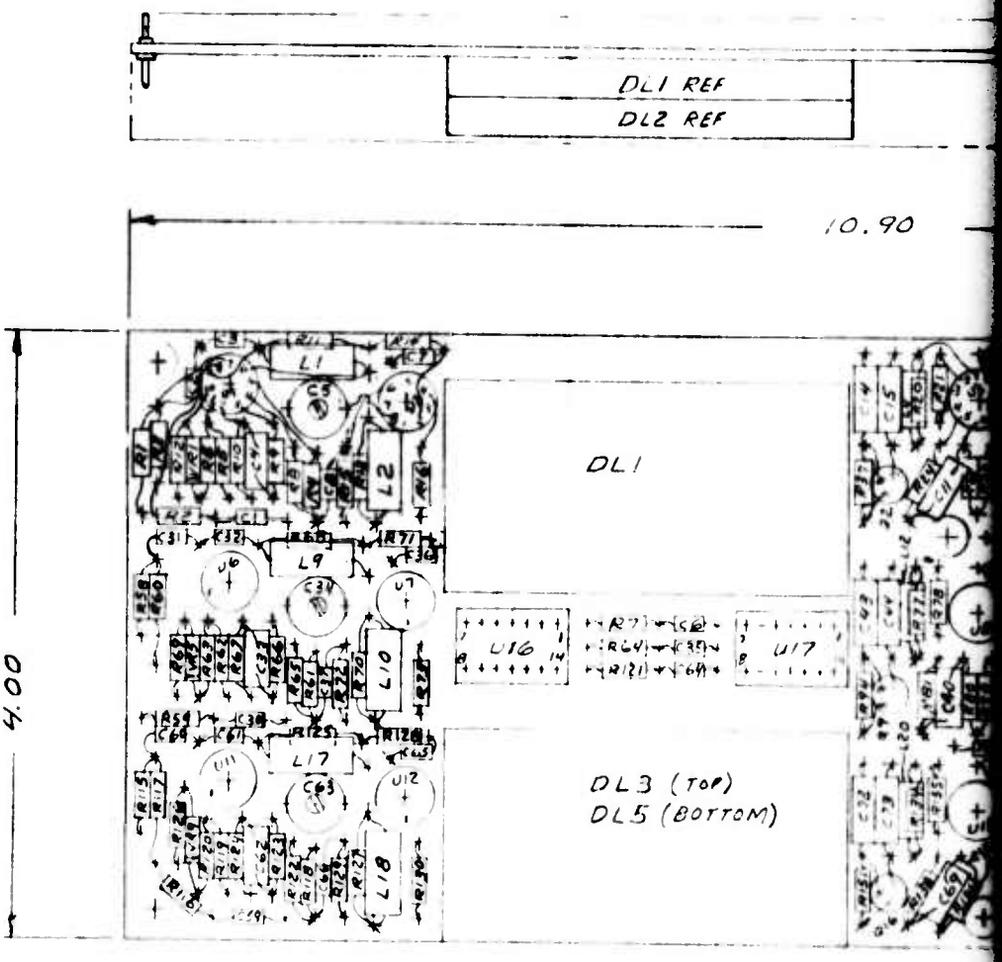
COMPONENTS LOCATED ON NS

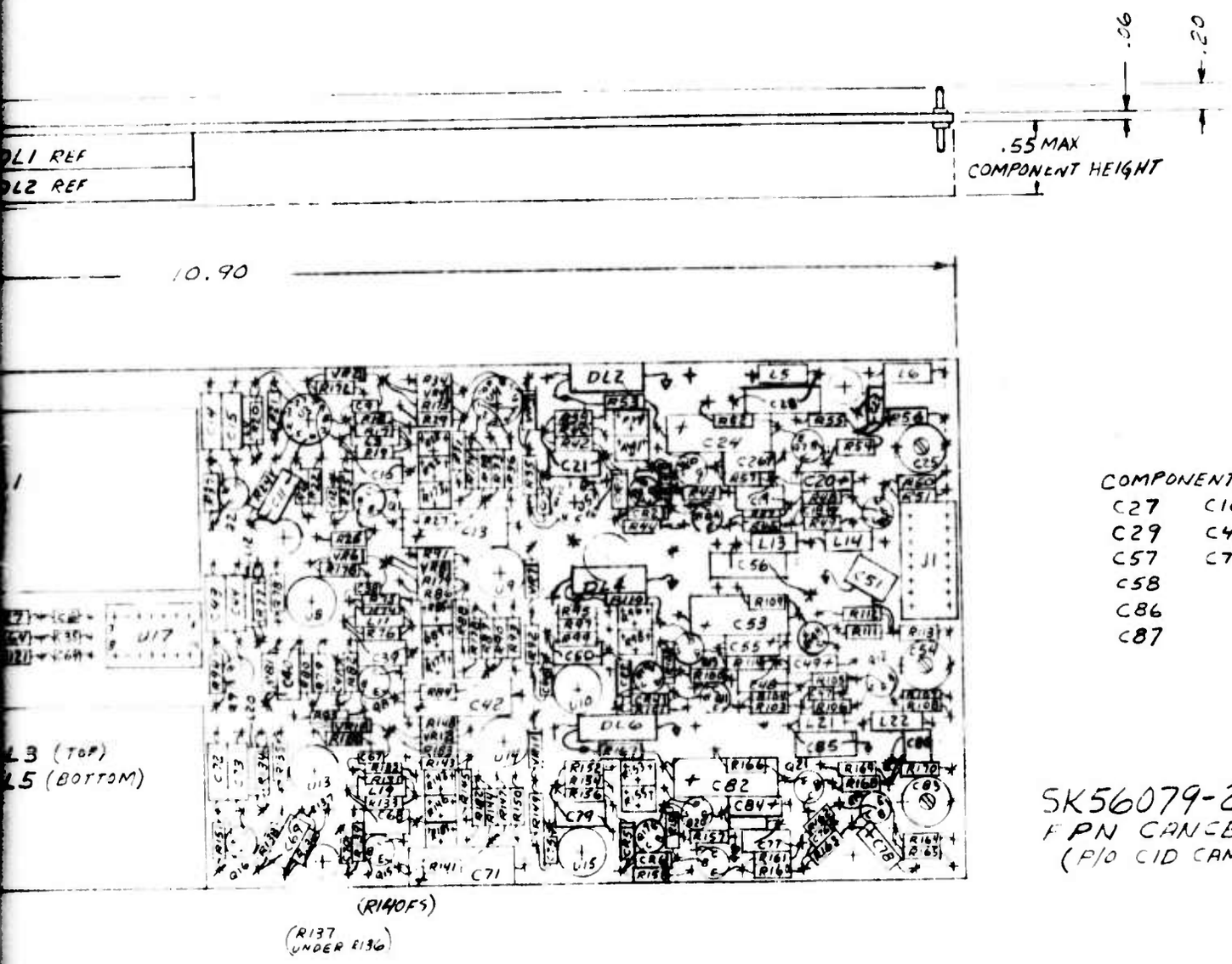
	FROM	TO
R92	R25-N	WT1
R93	R26-S	WT1
R96	R85-N	WT3
R97	R86-S	WT3
C19	R1-N	R7-S (GND)
C20	R2-S	R8-N(GND)
C42	R31-S	R37-N (GND)
C43	R32-N	R38-S(GND)
C65	R61-N	R67-S(GND)
C66	R62-S	R68N(GND)
R94	R37-S	WT4
R95	R38-N	WT4

PRE-AMPLIFIER
P/O SIC CAMERA
SK56079-21-20

Figure 5-3. Preamplifiers Assembly Drawing (SK56079-21-20)

B


DL1 REF
DL2 REF
10.90
4.00
L1
L2
L9
L10
L17
L18
U6
U7
U11
U12
U16
U17
DL1
DL3 (TOP)
DL5 (BOTTOM)



COMPONENTS ON FS

C27	C16
C29	C45
C57	C74
C58	
C86	
C87	

SK56079-21-23
FPN CANCELER
(P/O CID CAMERA)

Figure 5-4. FPN Canceller Assembly Drawing (SK56079-21-23)

B

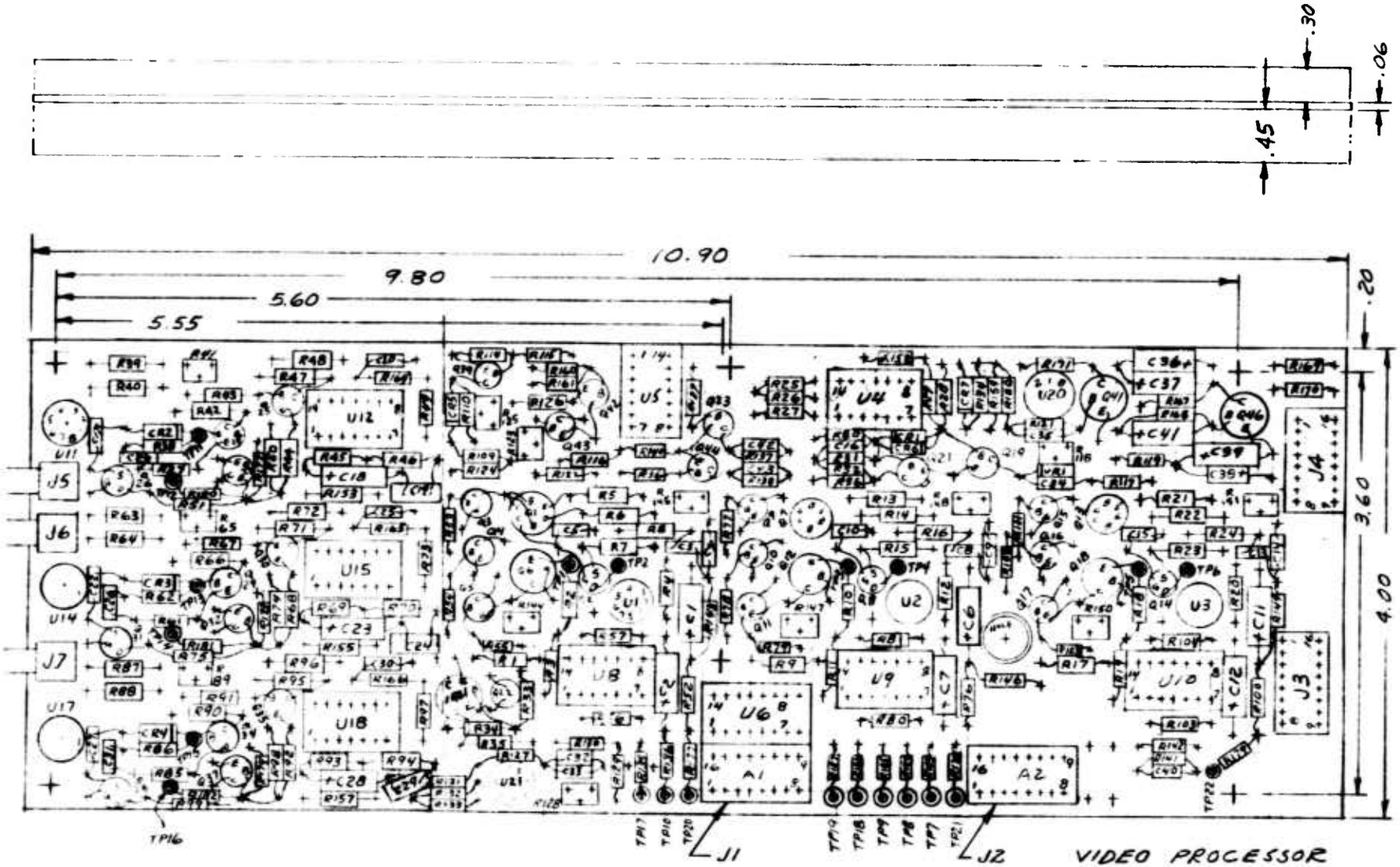


Figure 5-5. Color Processor Assembly Drawing (SK56079-21-21)

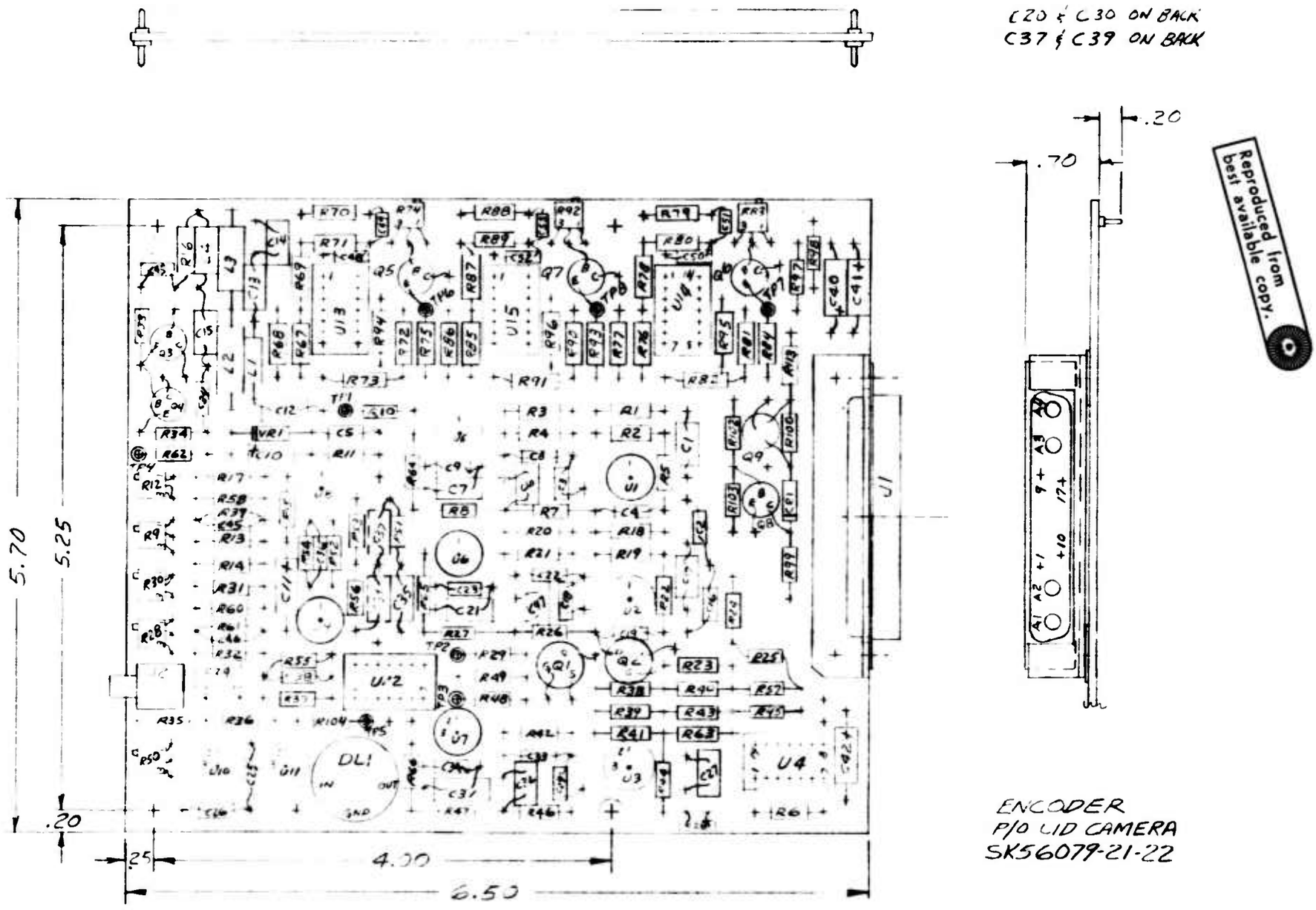


Figure 5-6. Encoder Assembly Drawing (SK56079-21-22)

APPENDIX 1

RANDOM ADDRESSING OF THE CID IMAGER

A1-1. INTRODUCTION

The following discussion will be concerned with design consideration and performance projections for CID imager configurations in which the signal charge at each sensing site is directly accessible for sensing and/or injection without regard to its physical location or time sequence with respect to other sites in the array. The term "random access" is commonly used in the computer field to describe this feature and so will be retained here. Random, i.e., haphazard, image readout is not to be inferred from the use of this terminology.

The X-Y coincident voltage configuration of the CID array makes it uniquely adaptable to the random address mode of operation; indeed, many of the decoding techniques developed for accessing MOS digital memories can be applied to random access imaging.

Image site selection differs from memory site selection in two important aspects, however. These are 1) a much higher dynamic range is required of the readout signal, and 2) variations in integration times between sensing sites due to non-sequential readout sequences must be accommodated.

A1-2. SELECTION TECHNIQUES

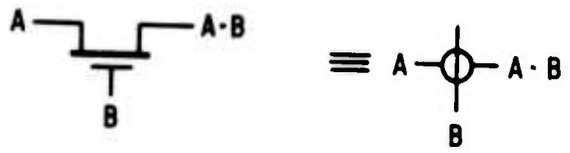
The charge injection image sensor consists basically of a two dimensional array of sensing sites configured for coincident voltage readout selection. Present self-scanned sensors utilize two sequential shift registers, one each for row and column selection, to effect a raster scan. There is no constraint, however on the order of scanning inherent in the charge injection structure. Any selection means that satisfies the coincident voltage readout conditions could be used. In order to mechanize a truly random scan, in which any sensing site in an array can be read out at any time, row and column selection decoders are

required. Decoding techniques that have been developed for MOS random access digital memory arrays can be applied to random scan-charge injection imagers.

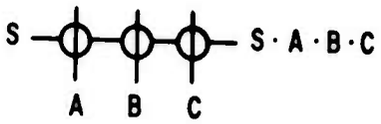
The advent of the MOS random access memory has led to the development of various MOS array line selection techniques. In general, decoder parameters required for a memory application are also desirable for random image sensor scanning. High speed, low power consumption, minimum package pin count, and circuit simplicity are desirable for both applications. MOS array selection techniques have previously been developed at General Electric [1,2]. The results of this work have been reviewed considering the specific requirements of the charge injection imager.

In order to obtain good drive voltage interference cancellation, a decoder for imaging application must allow good drive waveform control. This requirement alone practically limits the decoding circuitry to series AND gate configurations in which an externally applied drive waveform is transmitted to the selected array line. The series MOS AND gate is shown in Figure 1 along with a device symbol that will be used in the following discussion. Note that when the AND gate shown in Figure 1 is conducting, the S input is connected to the output.

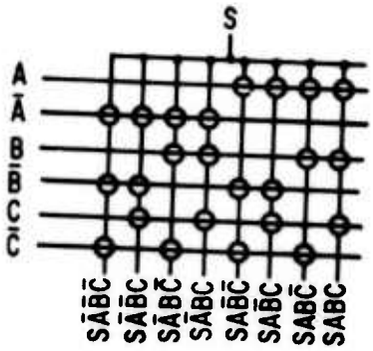
The two principle types of series MOS decoders are Binary and Combinatorial. A rectangular, one-of-eight binary series decoder is diagrammed in Figure 1c. The three binary address inputs (A, B, C) and their complements ($\overline{A}$, $\overline{B}$, $\overline{C}$) are required. On-chip inverters could be used to generate the address complements from the true inputs but at the cost of increased power consumption and decreased speed.



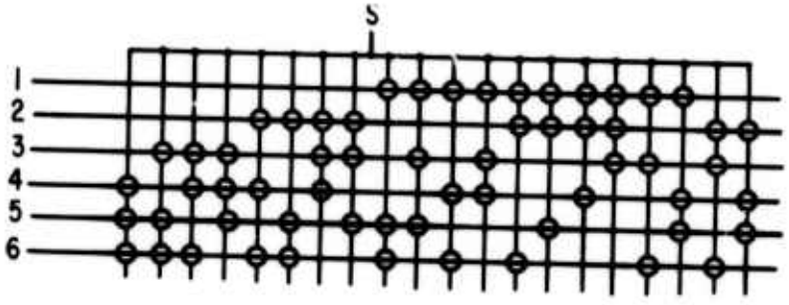
A. SINGLE MOSFET AND GATE.



B. 3 BOOLEAN INPUT AND GATE WITH SIGNAL INPUT.



C. RECTANGULAR MINTERM MATRIX.



D. RECTANGULAR COMBINATORIAL SERIAL ARRAY.

Figure 1. MOS Series Decode Logic

A1-2. (Continued)

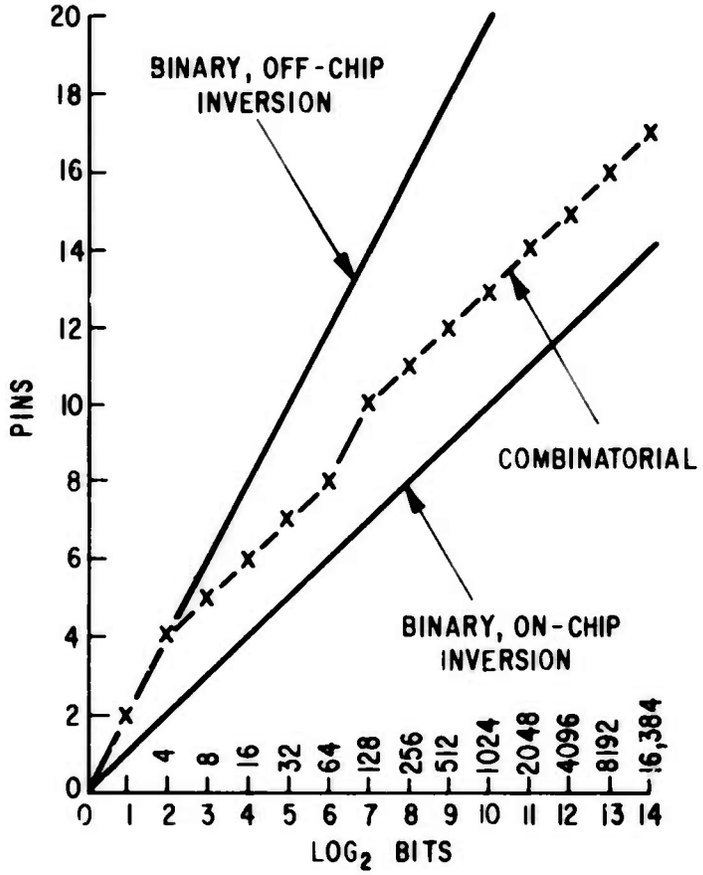
A three-of-six series combinatorial decoder is diagrammed in Figure 1d. In this decoder, three of the six address inputs select one-of-20 output lines. There are no on-chip inversions required but an external code converter is required to convert a binary address to a combinatorial address.

The pin count and gate complexity of combinatorial and binary series decoders are plotted as a function of size in Figure 2, for purposes of comparison.

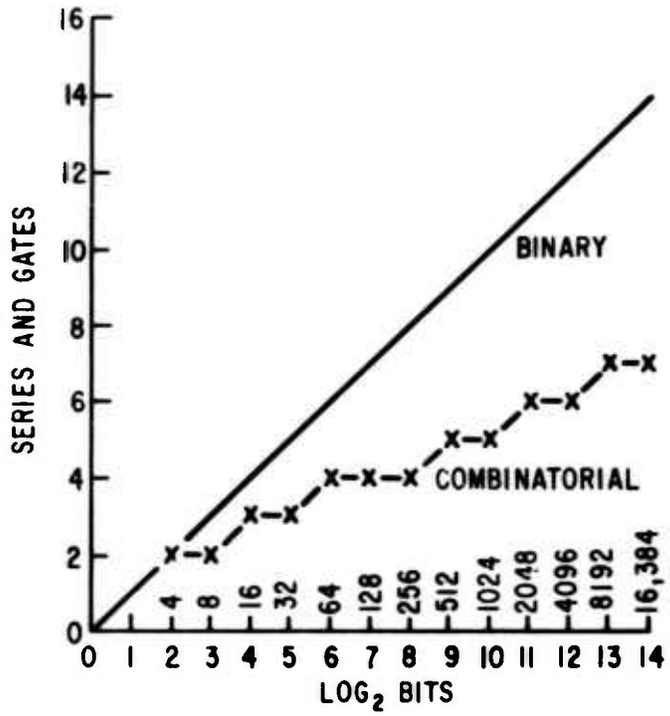
The additional factors that must be considered in this comparison are the significant speed loss encountered with on-chip inversion (binary), and the added system complexity resulting from the use of a code converter (combinatorial).

A choice of a decoding method for any specific application is, of course, dependent upon the performance requirements of the application. Highest speed and minimum on-chip complexity can be obtained by using combinatorial MOS decoders and high speed (TTL) code conversion electronics; low speed requirements could best be met through the use of binary selection matrices with on-chip inversion. For high speed selection, the on-chip drive line impedances must be considered in the design of the selection circuitry.

A 128 x 128 fully decoded array was designed to provide a basis for performance calculations. This array is shown schematically in Figure 3. Each axis is segmented into two 4-of-8 combinatorial decoders with eight combinatorial address lines servicing each axis. Thus for each combinatorial address, two columns (rows) are accessible. One is selected by a one-of-two decoder by means of the two address inputs. Since each decoder is capable of seventy



A. PIN COUNT vs THE NUMBER OF BITS SELECTED.



B. NUMBER OF SERIES GATES vs THE NUMBER OF BITS SELECTED.

Figure 2. Binary and Combinatorial Decoder Comparison

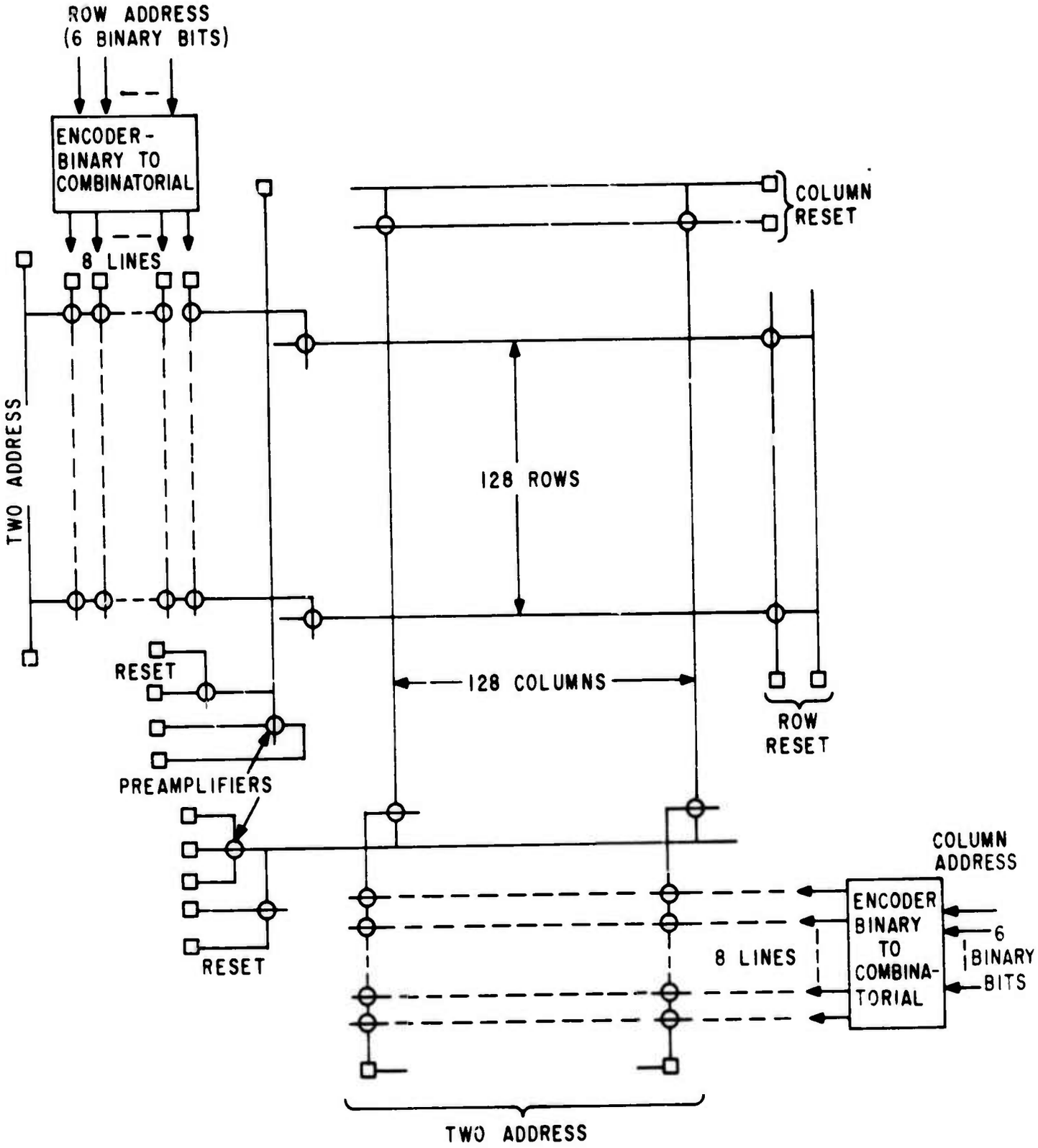


Figure 3 128 X 128 Random Access Array Schematic Diagram

A1-2 (Continued)

outputs ($_8C_4$= 70), there are six redundant codes. Reduction to 64 output lines was done by elimination of those lines with the highest impedance. By this means and by paralleling nodes within the decoder layout, the worst case series path impedance has been reduced to the equivalent of slightly more than three transistors in series.

The encoding function can be done by means of a 128-bit bipolar PROM (1M5600, for example). Two PROM's are required per axis. This approach permits much greater ease of coding and greatly reduced package count over other available means although it involves a slight speed penalty.

A1-3. PERFORMANCE

Since the only fundamental difference between the random access mode of operation and the sequential modes previously employed is in the site selection technique, it follows that the major performance difference will be in the speed of response. For this reason, the following analysis emphasizes this feature.

As with the sequential readout approach, two modes of operation are possible - sequential injection, in which the signal charge is injected for sensing; and parallel injection, in which the injection function is deferred to a later time in the cycle. The latter approach allows a much faster pixel rate, provided that the system timing includes a convenient time slot for injection at a later time.

Sequential injection, while basically slower due to the addition of the injection and recovery time to each readout, is significantly superior to deferred injection in pattern noise performance since the readout is basically differential in nature.

A1-3 (Continued)

For convenience in the following discussion data for non-destructive readout (NDRO), i.e., no injection, will be presented first and the effects (and implications) of injection will be discussed later.

1. Response Time, NDRO

The response time for completely random scan has been calculated to obtain an estimate of maximum operating speed. Row and column address encoding can occur in parallel. The addressed row, however, must be switched before the resultant change in column voltage can be sensed. Since the polysilicon row or column lines would be used, the response time of the resultant distributed RC transmission lines must be considered. Figure 4 shows the calculated rise times for an open-ended polysilicon line (10Ω /□) for the 128 x 128 imager. The lower curve is for a column, with the charge stored under the row electrode. Note that for a 1.5 mil site this time is about 25 nanosec.

Total response time can be estimated from the known encoder/driver delay time and a calculated decoder and selection transistor time constant. The worst case decode delay occurs with three decode transistors in series as indicated in Figure 5. This time constant is about 15 nsec (30K series decode resistance and 0.5 pf load capacitance). Since the selection transistor is driving this row line toward ground, row switching will begin before the decoder has completely switched its output voltage. A reasonable value for the decode delay is 10 nsec. Charge would be stored under the row electrode which should be high conductance (metal) to minimize system access time. Row switching time would be determined by the selection transistor on-resistance and row capacitance. The calculated value for a 1.5 x 1.5 mil sensing site are 1K-Ω and 15 pF respectively. The row switching time would be about

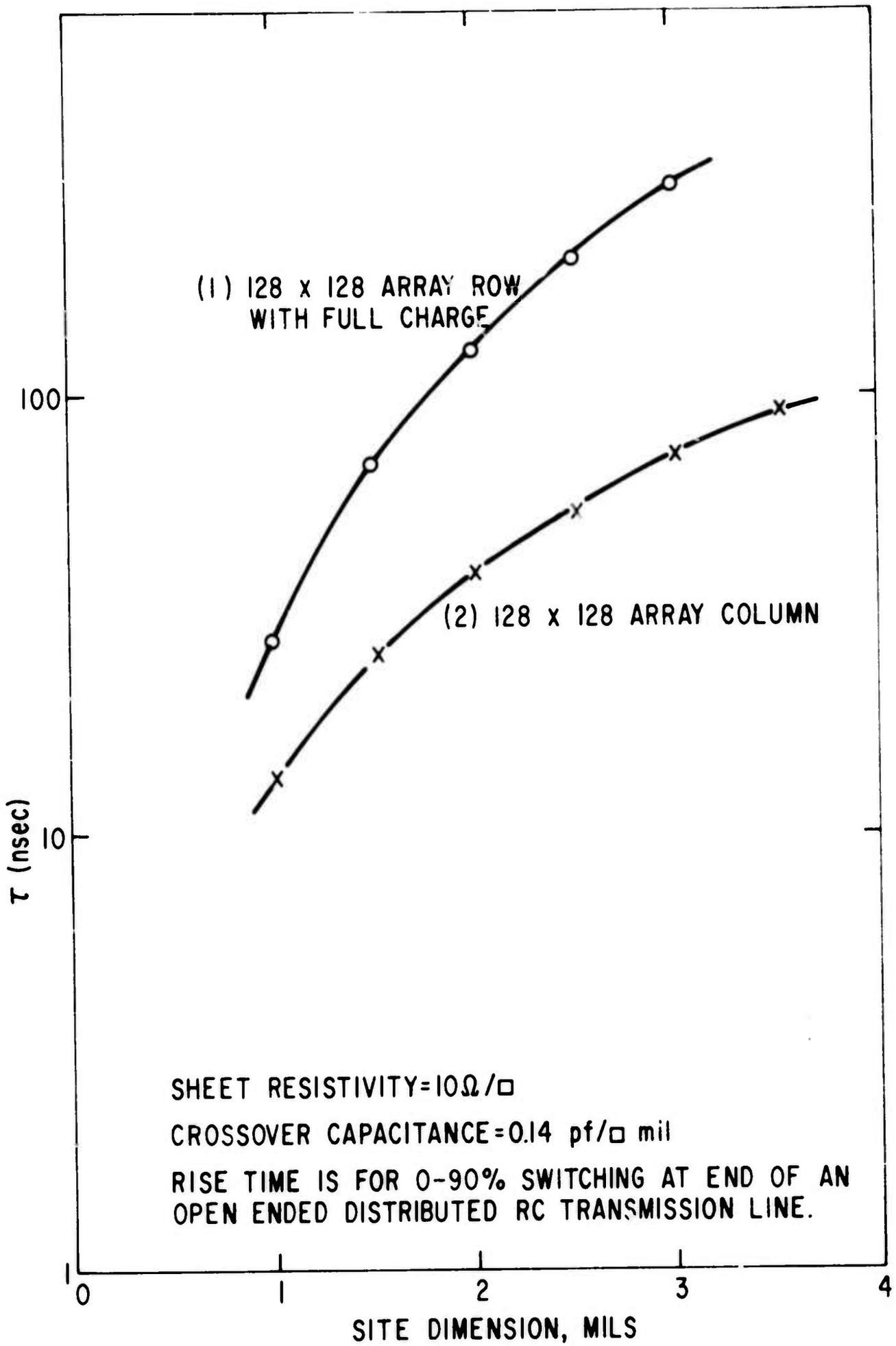


Figure 4. Polysilicon Response VS Site Size

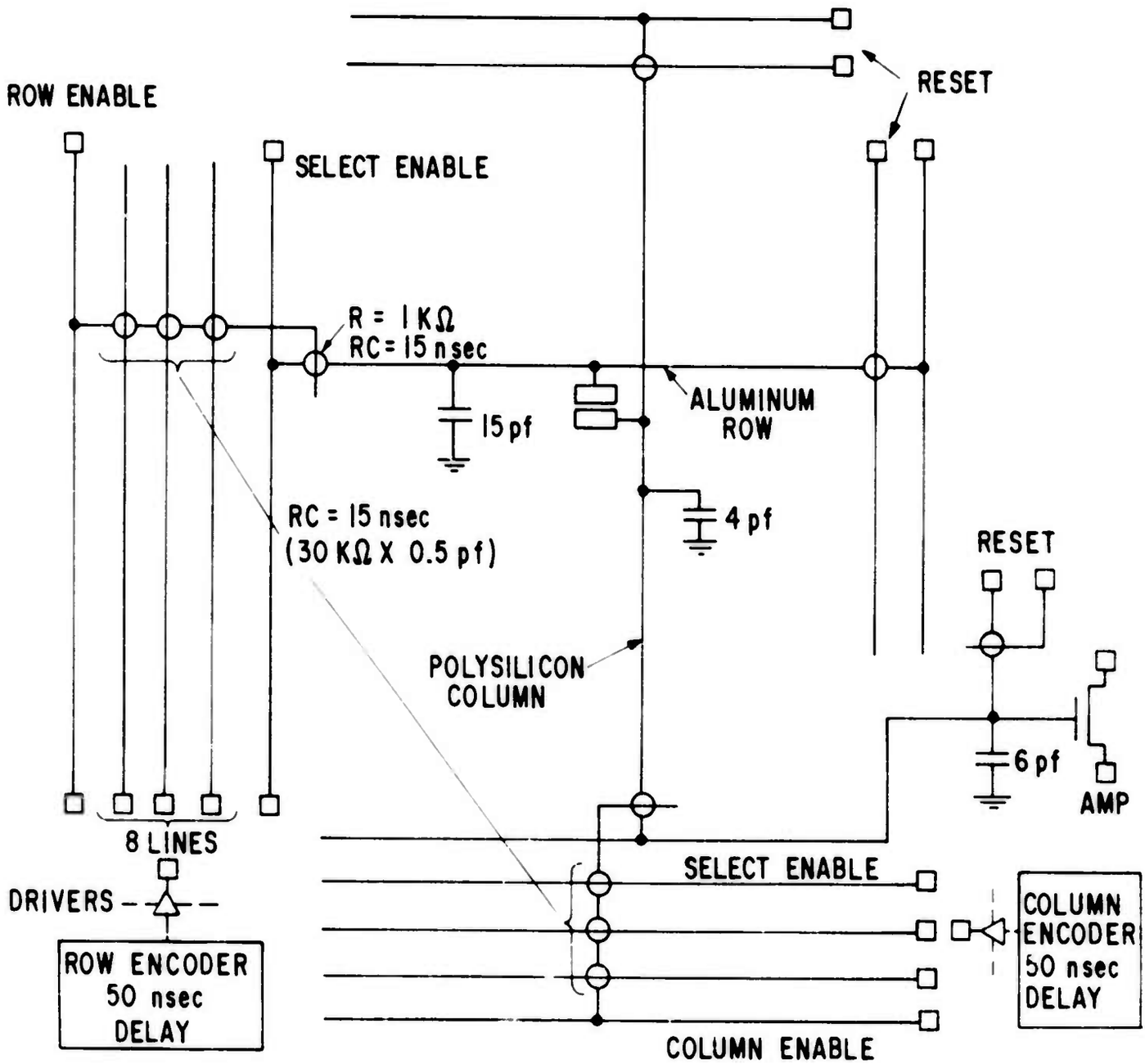


Figure 5. Response Time Estimates 128 x 128 Array

A1-3 (Continued)

3 time constants. Column response time would be determined by the distributed RC transmission line response of the poly column lines (Figure 4) since the solumn selection time constant (1K-Ω x 4 pF = 4 nsec) is very small. This assumption may involve some error, since the column lines in this case are not open-ended as indicated in Figure 4, but in fact are loaded by the RC series load of the column selection switches and enable line capacitance.

There remains a sampling time interval of arbitrary lengtn. For this calculation, fifty nanoseconds is assigned to this function. In practice, this time should be set as long as possible to reduce video bandwidth and hence noise.

Following sampling, row and column voltages must be restored to their preselection values before initiating another site address cycle. Figure 6 shows how the various events occur in a readout cycle. Note that a considerable time saving can be effected by time overlap of some events so that a maximum data rate of about 210 nsec/pixel appears possible for the 128 x 128 array for fully random access operation, exclusive of injection time. To extrapolate, this result to a 256 x 256 array, assuming no change in array layout, one must double the row and quadruple the column response times. This is because the row RC product would vary linearly with array linear dimension while the distributed RC column response time varies as the length squared (L^2). This has the effect of adding 45 + 75 = 120 nsec to the above total to give about 330 nsec cycle time for the larger array.

2. Charge Injection

The specific method of charge injection best suited to random scanning will largely depend on system considerations. Sequential injection, in which the charge at each site is injected as part of the readout process, could

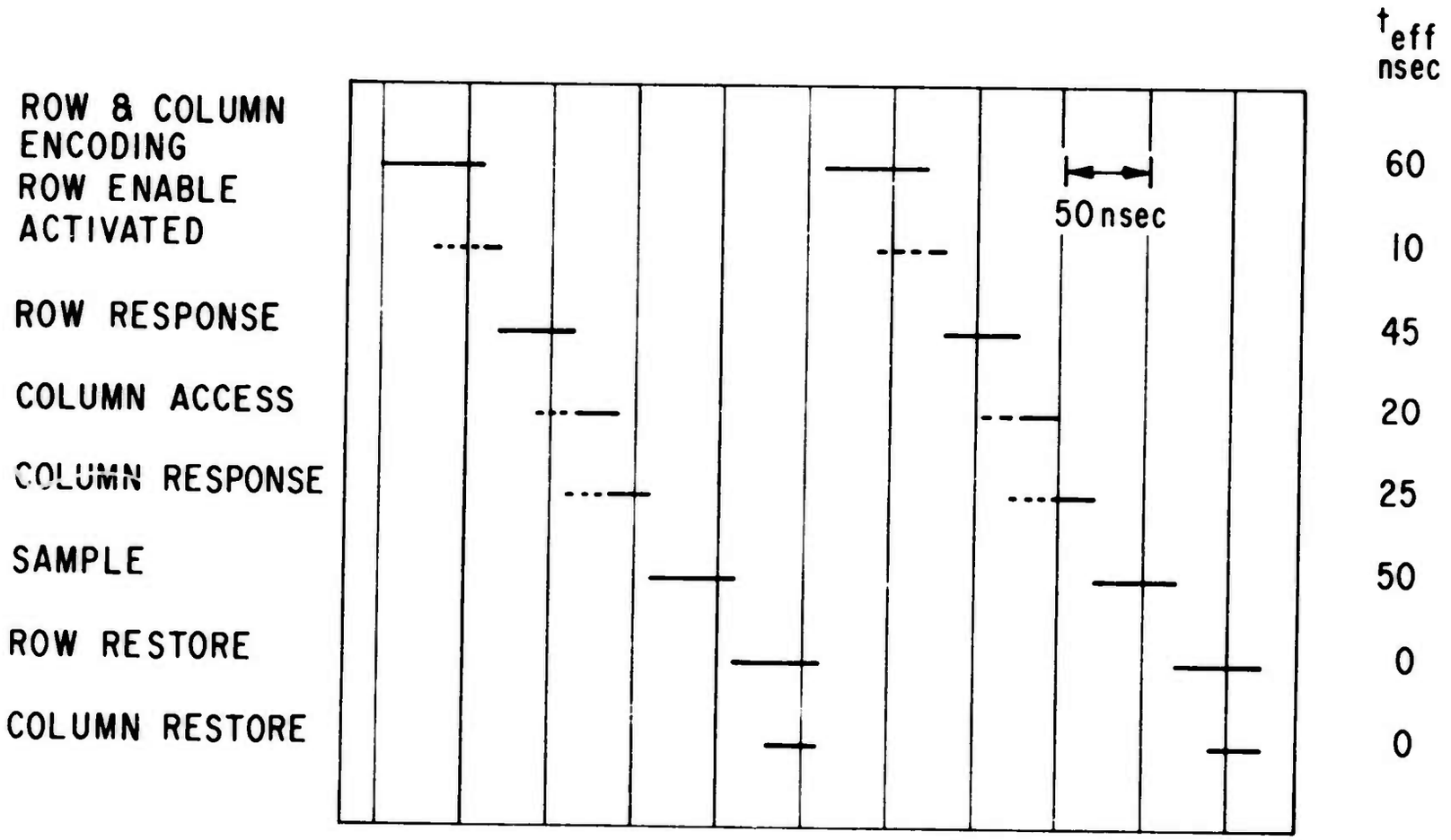


Figure 6. Sequence of Events During Cycle Time For Fully Random Address Array. (Polysilicon Column, Aluminum Row.)

A1-3. (Continued)

be rather easily mechanized to constant integration-time imaging as it would only be required that the site selection pattern repeat frame-to-frame. This method slows the readout process, however, and of course is destructive to the image information. The time required to inject the charge from a single site has two parts; 1) the time for collection and/or recombination of the inject charge, and 2) system recovery time from drive disturbances introduced during injection. The first effect is well understood and predictable. Calculations and measurements verify that essentially all of the injected charge can be disposed of in about 100 nsec for the conditions currently employed for sequential imaging. Unfortunately, sense system recovery time cannot be accurately specified, as it is largely dependent on specific array and amplifier circuit design, which depend in turn upon system requirements.

Also note that for the array as described above injection must be done by driving the polysilicon columns. This introduces additional delay since it sets the minimum injection pulse width at something like 300 nsec. A reasonable guess for system recovery is an additional 200 nsec. Thus a full pixel time for a 256 x 256 array, including injection and recovery, would probably be about 330 + 500 = 830 nsec for an effective frame rate of about 20 frames/sec.

For frame rates higher than about 20 fps, therefore, some form, of parallel injection is indicated, either by row (columns) or by blocks. Specific methods would depend on the particular system involved. The above result is slightly pessimistic in that it is an extrapolation from results from the smaller (128 X 128) array. In that array, for instance, a site size of 1.5 mils was chosen to match the polysilicon column response to that of the decoder.

A1-3 (Continued)

This is because the width, and hence the conductance of the decode transistors is proportional to the line repeat dimension. For the larger array, a smaller site size might well be chosen, resulting in a sizeable reduction in the row response time (the term "might" is used here advisedly, since many other considerations influence the choice of site size).

A1-4. CONCLUSIONS:

Random Accessing of the CID imager is quite feasible and while performance cannot be precisely specified without a complete list of system requirements, it appears that a 256 X 256 RACID could be built to operate at about 1 MHz pixel rate using sequential injection and considerably faster during NDRO. Higher resolution arrays (to 512 X 512 say) are technically possible to design and fabricate at the present time. Fabrication of such large arrays, while difficult at the present state of the silicon processing art, will surely be quite practical in the near future.

D. References

1. W.D. Barber, "MOS Memory Array Selection" General Electric Company Report #70-C-334, October 1970.

2. H.K. Burke and G.J. Michon, "Charge Pump Random Access Memory" 1972 IEEE International Sold-State Circuits Conference Digest, Pages 16-17.

APPENDIX 2

TEST RESULTS

A2-1 INTRODUCTION

The testing on the CID Color Camera consisted of engineering proof testing over a temperature range of -20°C to +55°C. The results of the tests follow.

A2-2 COLOR PROCESSOR TESTS

The color processor was tested as an engineering breadboard, and included the gamma correctors. Test results reported here include the gamma corrector, unless noted otherwise.

Input levels are referenced to 0 db as 200 mv peak-peak.

The following parameters were measured at 25°C ambient temperature with identical inputs to the three channels;

Bandwidth (3 db) to gamma corrector input — 4.2 MHz

AGC range (input) — 40 db min

Tracking:

INPUT LEVEL DB	OUTPUT (VOLTS) RED	GREEN	BLUE	TRACKING (MIN/MAX)
0	0.215	0.203	0.218	0.931
-10	0.206	0.212	0.218	0.945
-20	0.218	0.221	0.215	0.973
-30	0.221	0.212	0.206	0.932
-40	0.212	0.212	0.206	0.972

A2-2 (Continued)

The breadboard was tested over a temperature range of -20°C to +55°C to verify proper operation. Bandwidth remained at 4.2 MHz. The output level was maintained over the 40 db range of inputs.

The tracking and match of the gamma correctors were monitored by making a subjective assessment of a stairstep waveform on the monitor. The displayed stairstep remained acceptably gray over the temperature range at each input level (0, -10, -20, -30, and -40 dB) for each step above 10%. The 10% step was a low saturation Blue at 0 db input level.

A2-3 ENCODER TESTS

The following parameters were measured on the final subassembly at 25°C ambient temperature:

1) Luminance Channel Bandwidth

   (3 dB, from Green input to output) 2.85 MHz

2) Chroma Channel Attenuation

   R-Y (Red input to modulator) 4.68 db

   B-Y (Blue input to modulator) 2.98 db

3) Luminance Levels (75% Color Bars, IRE Units) Figure 1:

COLOR	MEASURED	STANDARD
White	77	77 ± 2 IRE
Yellow	68	69 ± 2 IRE
Cyan	54	56 ± 2 IRE
Green	46	48 ± 2 IRE
Magenta	38	36 ± 2 IRE
Red	29	28 ± 2 IRE
Blue	16	15 ± 2 IRE
Black (setup)	7.5	7.5 ± 2 IRE

4) Chroma Error; each

Color Bar (Figure 2) ≤ 2.5 IRE

$\leq 2.5^{o}$

Temperature tests were made on the engineering breadboard to verify operation over the range -20°C to +55°C. The luminance levels and chroma vectors were monitored over the range and are shown in Figures 3 and 4. The circuit remained within less than ± 2 IRE drift in luminance levels. The chroma vectors remained within ± 2.5 IRE amplitude and $\pm 2.5^{o}$ angle.

A2-4 DRIVERS AND PREAMPLIFIER TESTS

The drivers, preamplifier and a CID imager were tested together through a temperature range of -20°C to +60°C. The results are given in Table 1. The interference level in the table was measured on a single line of video, and neglects fast transients at the multiplex transitions. The output offset shows a definite drift with temperature. This is predominantly due to the increase in dark current with temperature. The saturation signal level decreases with temperature also due to the increase in dark current.

A2-5 CANCELER TEST

A single channel of the final canceler subassembly was adjusted for maximum cancellation at an ambient temperature of 25°C and tested over a temperature range of -20°C to +60°C. Cancellation was measured as a function of frequency by applying a 200 mv p-p full field multiburst to the canceler input, and observing the output for the first and second lines of multiburst.

A2-5 Canceler Test (Continued)

The first line is thus uncancelled, and shows the frequency response of the undelayed channel. The second line is cancelled. The cancellation ratio is defined as

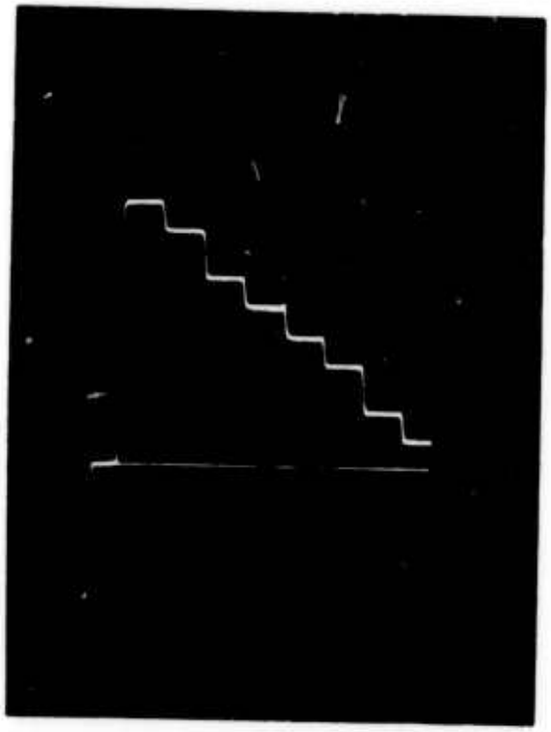
$$\text{cancellation ratio} = 20 \log \frac{\text{uncancelled}}{\text{cancelled}}$$

Table 1. Drivers and Preamplifier Test Results

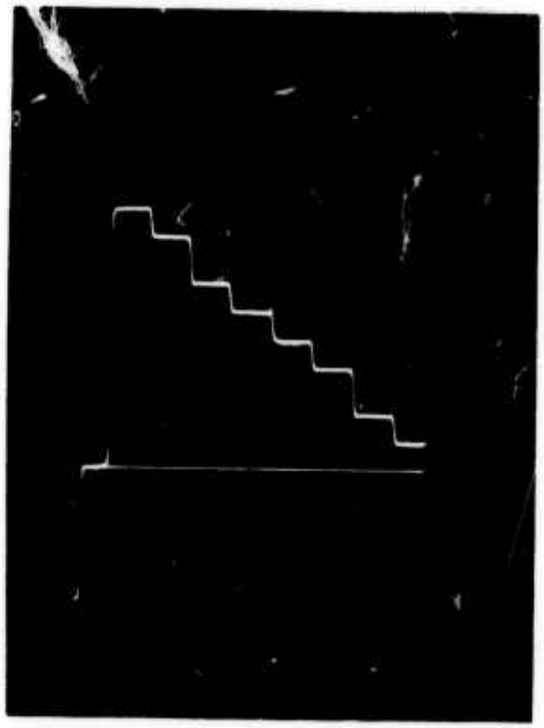
TEMPERATURE	INTERFERENCE (MVPP)	OUTPUT OFFSET (MV)	SATURATION SIGNAL LEVEL OUT (MV)
-20	20	+140	80
0	10	+135	80
+25	10	+175	80
+40	25	+230	60
+60	30	+400	40

Figure 1. Luminance Levels (75% Color Bars), Final Subassembly

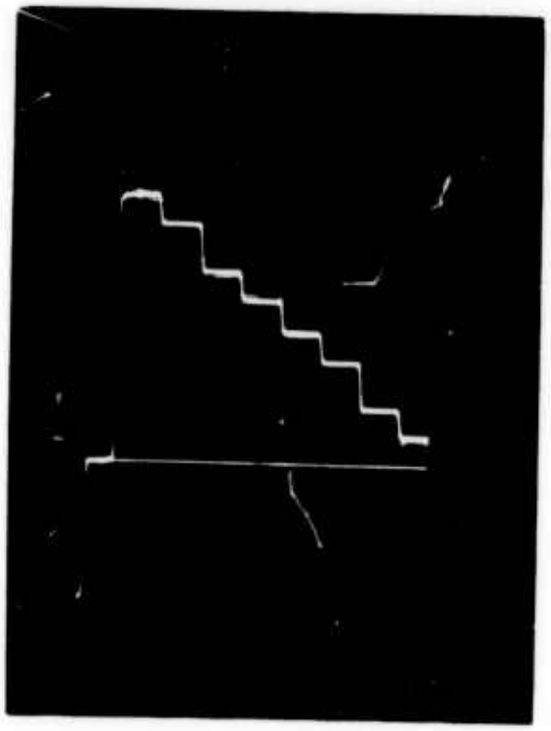
Figure 2. Chroma Vectors, Final Subassembly



a) +25°C

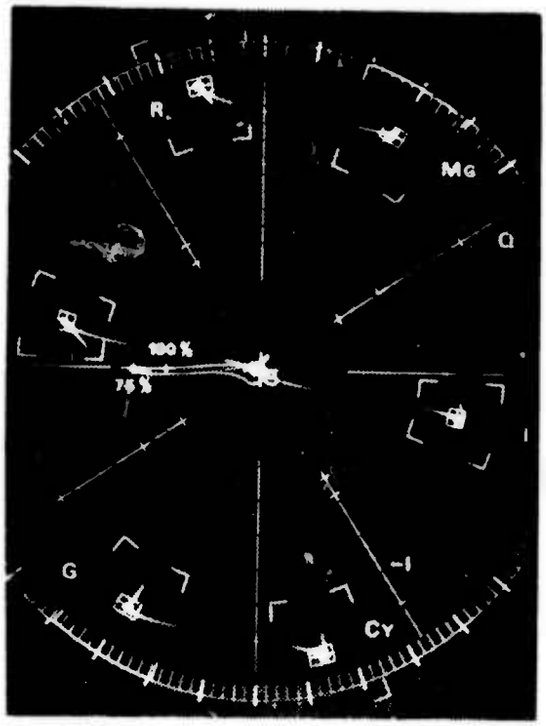


b) +55°C (20 min)

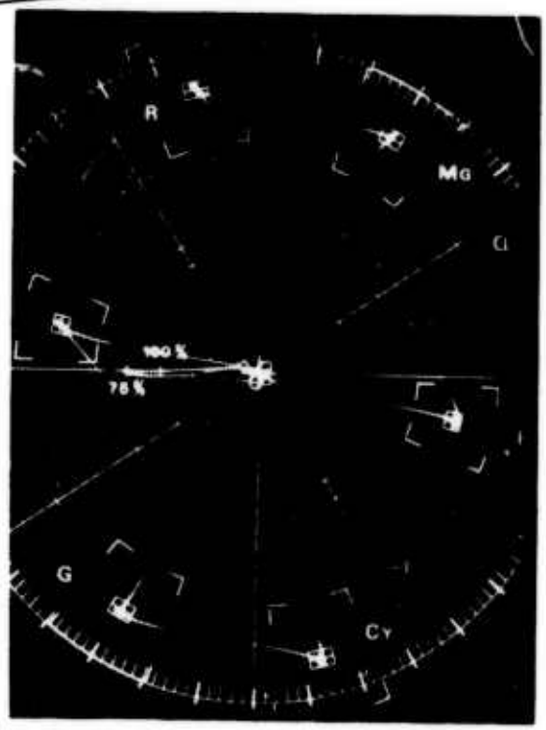


c) -20°C (28 min)

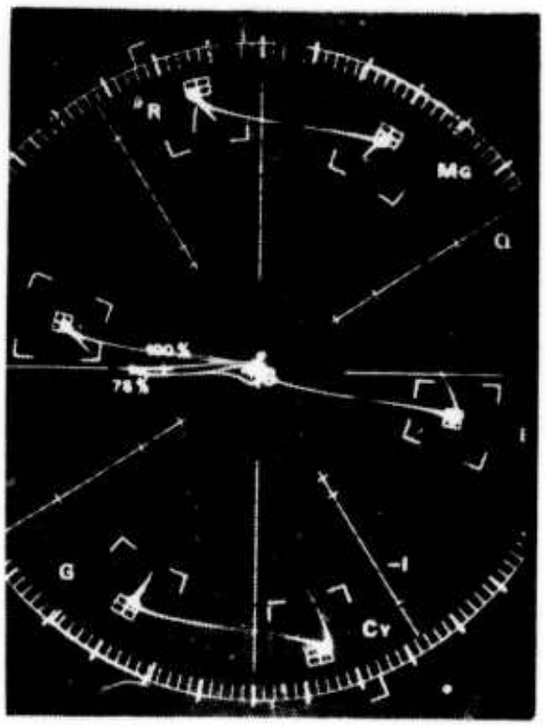
Figure 3. Breadboard Temperature Tests, Luminance Levels



a) 25°C



c) +55°C (20 min)



c) -20°C (28 min)

Figure 4. Breadboard Temperature Tests, Chroma Vector

A2-5 (Continued)

The measured cancellation ratio as a function of frequency and temperature is given in Table 2.

The cancellation is less than desired at low temperatures. This is due to a variation in the gain of the 1h delay line with temperature. For example, if the gain of the delay line decreases by 32%, the maximum cancellation possible is 9.9 db, assuming optimum nominal adjustment. The transducer on the quartz delay line changes gain with temperature.

The 3 db bandwidth was measured as 2.2 MHz.

Table 2. Canceler Test Results

TEMPERATURE (°C)	CANCELLATION RATIO (DB) 0.5 MHZ	1.5MHZ	2.0MHZ
60	21.6	11.28	18.8
40	23.2	16.9	22.3
25	25	19.4	22.3
0	14.0	13.1	19
-20	9.3	9.54	14.3